Pro WS sTR5 Series

BIOS Manual

Motherboard

E22761
First Edition
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Contents

BIOS Setup

1. Knowing BIOS

BIOS (Basic Input and Output System) stores system hardware settings such as storage device configuration, overclocking settings, advanced power management, and boot device configuration that are needed for system startup in the motherboard CMOS. In normal circumstances, the default BIOS settings apply to most conditions to ensure optimal performance. **DO NOT change the default BIOS settings** except in the following circumstances:

- An error message appears on the screen during the system bootup and requests you to run the BIOS Setup.
- You have installed a new system component that requires further BIOS settings or update.

Inappropriate BIOS settings may result to instability or boot failure. **We strongly recommend that you change the BIOS settings only with the help of a trained service personnel**.

- When downloading or updating the BIOS file for your motherboard, rename it as **XXXXX.CAP** or launch the **BIOSRenamer.exe** application to automatically rename the file. The name of the CAP file varies depending on models. Refer to the user manual that came with your motherboard for the name.
- The screenshots in this manual are for reference only, please refer to the latest BIOS version for settings and options.
- BIOS settings and options may vary due to different BIOS release versions or CPU installed. Please refer to the latest BIOS version for settings and options.

2. BIOS setup program

Use the BIOS Setup to update the BIOS or configure its parameters. The BIOS screen include navigation keys and brief onscreen help to guide you in using the BIOS Setup program.

Entering BIOS at startup

To enter BIOS Setup at startup, press <Delete> or <F2> during the Power-On Self Test (POST). If you do not press <Delete> or <F2>, POST continues with its routines.

Entering BIOS Setup after POST

To enter BIOS Setup after POST:

- Press <Ctrl>+<Alt>+<Delete> simultaneously.
- Press the reset button on the system chassis.
- Press the power button to turn the system off then back on. Do this option only if you failed to enter BIOS Setup using the first two options.

After doing either of the three options, press <Delete> key to enter BIOS.

- The BIOS setup screens shown in this section are for reference purposes only, and may not exactly match what you see on your screen.
- If the system becomes unstable after changing any BIOS setting, load the default settings to ensure system compatibility and stability. Select the **Load Optimized Defaults** item under the **Exit** menu or press hotkey **<F5>**. See section **Exit menu** for details.
- If the system fails to boot after changing any BIOS setting, try to clear the CMOS and reset the motherboard to the default value. See your motherboard manual for information on how to erase the RTC RAM.
- The BIOS setup program does not support Bluetooth devices.

3. Managing and updating your BIOS

The following utilities allow you to manage and update the motherboard Basic Input/Output System (BIOS) setup:

1. ASUS CrashFree BIOS 3

   To recover the BIOS using a bootable USB flash disk drive when the BIOS file fails or gets corrupted.

2. ASUS EzFlash

   Updates the BIOS using a USB flash disk.

3.1 ASUS CrashFree BIOS 3 utility

The ASUS CrashFree BIOS 3 is an auto recovery tool that allows you to restore the BIOS file when it fails or gets corrupted during the updating process. You can update a corrupted BIOS file using a USB flash drive that contains the updated BIOS file.

Prepare a USB flash drive containing the updated motherboard BIOS before using this utility.

Recovering the BIOS from a USB flash drive

To recover the BIOS from a USB flash drive:

1. Insert the USB flash drive with the original or updated BIOS file to one USB port on the system.
2. The utility will automatically recover the BIOS. It resets the system when the BIOS recovery finished.

DO NOT shut down or reset the system while recovering the BIOS! Doing so would cause system boot failure!

The recovered BIOS may not be the latest BIOS version for this motherboard. Visit the ASUS website at www.asus.com to download the latest BIOS file.

3.2 ASUS EzFlash Utility

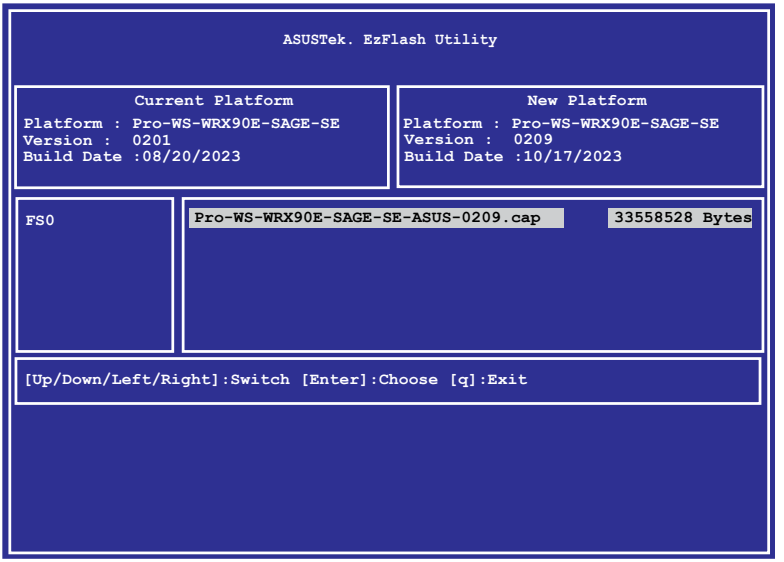
The ASUS EzFlash Utility feature allows you to update the BIOS using a USB flash disk without having to use a DOS-based utility.

Download the latest BIOS from the ASUS website at www.asus.com before using this utility.

The succeeding BIOS screens are for reference only. The actual BIOS screen displays may not be the same as shown.

To update the BIOS using EzFlash Utility:

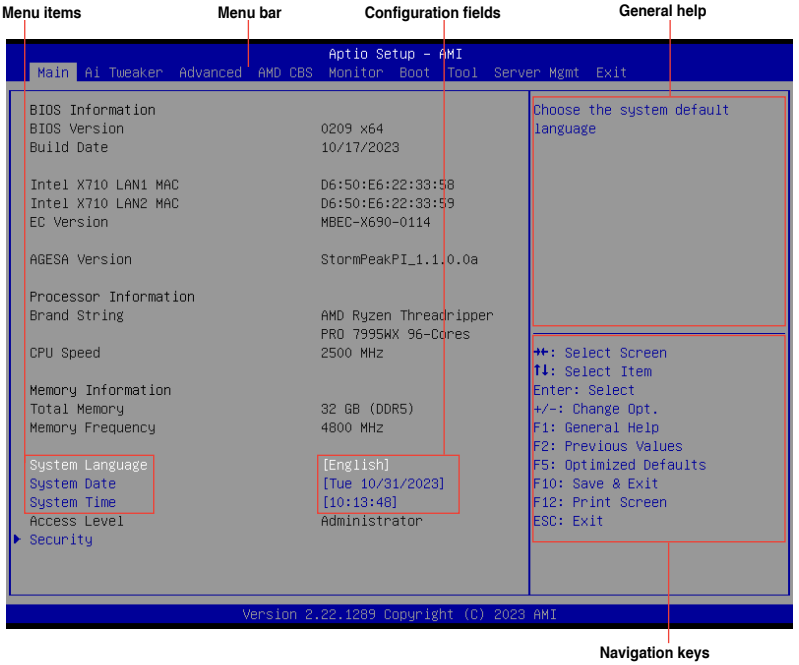
1. Insert the USB flash disk that contains the latest BIOS file to the USB port.
2. Enter the BIOS setup program. Go to the **Tool** menu to select **Start ASUS EzFlash** and press <Enter> to enable it.



3. Press the Left arrow key to switch to the **Drive** field.
4. Press the Up/Down arrow keys to find the USB flash disk that contains the latest BIOS then press <Enter>.
5. Press the Right arrow key to switch to the **Folder Info** field.
6. Press the Up/Down arrow keys to find the BIOS file then press <Enter>.
7. Reboot the system when the update process is done.

4. BIOS menu screen

The screenshot for this section is for reference only, and may vary between motherboards. Please refer to the actual BIOS of your motherboard.



4.1 Menu bar

The menu bar on top of the screen has the following main items:

Main	For changing the basic system configuration
Ai Tweaker	For changing the overclocking settings
Advanced	For changing the advanced system settings
AMD CBS	For configuring AMD CBS settings
Monitor	For displaying the system temperature, power status, and changing the fan settings
Boot	For changing the system boot configuration
Tool	For configuring options for special functions
Server Mgmt	For configuring IPMI options
Exit	For selecting the save & exit options

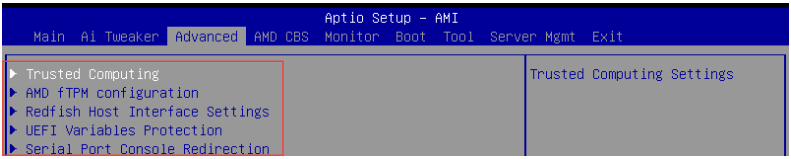
To select an item on the menu bar, press the right or left arrow key on the keyboard until the desired item is highlighted.

4.2 Menu items

The highlighted item on the menu bar displays the specific items for that menu. For example, selecting Main shows the Main menu items. The other items on the menu bar have their respective menu items.

4.3 Submenu items

A solid triangle before each item on any menu screen means that the item has a submenu. To display the submenu, select the item and press <Enter>.



4.4 Navigation keys

At the bottom right corner of a menu screen are the navigation keys for the BIOS setup program. Use the navigation keys to select items in the menu and change the settings.

4.5 General help

At the top right corner of the menu screen is a brief description of the selected item.

4.6 Configuration fields

These fields show the values for the menu items. If an item is user-configurable, you can change the value of the field opposite the item. You cannot select an item that is not user-configurable. A configurable field is enclosed in brackets, and is highlighted when selected. To change the value of a field, select it and press <Enter> to display a list of options.

4.7 Pop-up window

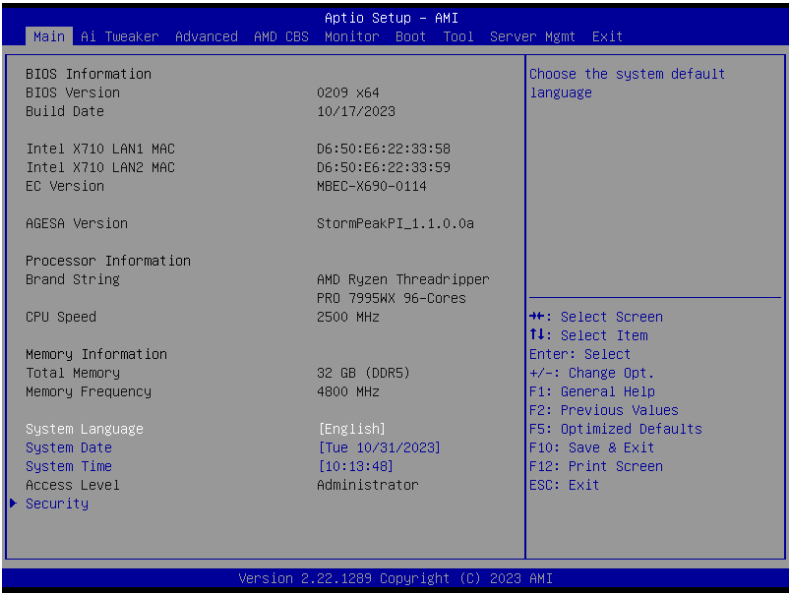
Select a menu item and press <Enter> to display a pop-up window with the configuration options for that item.

4.8 Scroll bar

A scroll bar appears on the right side of a menu screen when there are items that do not fit on the screen. Press the Up/Down arrow keys or <Page Up> /<Page Down> keys to display the other items on the screen.

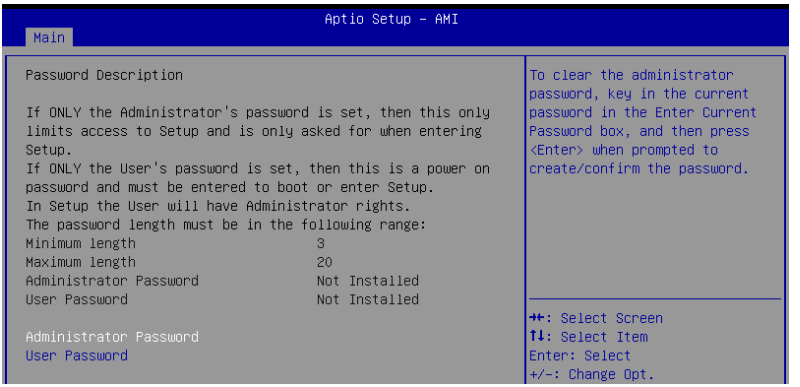
5. Main menu

The Main menu screen appears when you enter the Advanced Mode of the BIOS Setup program. The Main menu provides you an overview of the basic system information, and allows you to set the system date, time, language, and security settings.



Security

The Security menu items allow you to change the system security settings.



- If you have forgotten your BIOS password, erase the CMOS Real Time Clock (RTC) RAM to clear the BIOS password. See the motherboard for information on how to erase the RTC RAM via the Clear CMOS jumper.
- The Administrator or User Password items on top of the screen show the default **[Not Installed]**. After you set a password, these items show **[Installed]**.

Administrator Password

If you have set an administrator password, we recommend that you enter the administrator password for accessing the system. Otherwise, you might be able to see or change only selected fields in the BIOS setup program.

To set an administrator password:

1. Select the **Administrator Password** item and press <Enter>.
2. From the **Create New Password** box, key in a password, then press <Enter>.
3. Re-type to confirm the password then select **OK**.

To change an administrator password:

1. Select the **Administrator Password** item and press <Enter>.
2. From the **Enter Current Password** box, key in the current password, then press <Enter>.
3. From the **Create New Password** box, key in a new password, then press <Enter>.
4. Re-type to confirm the password then select **OK**.

To clear the administrator password, follow the same steps as in changing an administrator password, but leave other fields blank then select **OK** to continue. After you clear the password, the **Administrator Password** item on top of the screen shows **[Not Installed]**.

User Password

If you have set a user password, you must enter the user password for accessing the system. The User Password item on top of the screen shows the default **[Not Installed]**. After you set a password, this item shows **[Installed]**.

To set a user password:

1. Select the **User Password** item and press <Enter>.
2. From the **Create New Password** box, key in a password, then press <Enter>.
3. Re-type to confirm the password then select **OK**.

To change a user password:

1. Select the **User Password** item and press <Enter>.
2. From the **Enter Current Password** box, key in the current password, then press <Enter>.
3. From the **Create New Password** box, key in a new password, then press <Enter>.
4. Re-type to confirm the password then select **OK**.

To clear the user password, follow the same steps as in changing a user password, but leave other fields blank then select **OK** to continue. After you clear the password, the **User Password** item on top of the screen shows **[Not Installed]**.

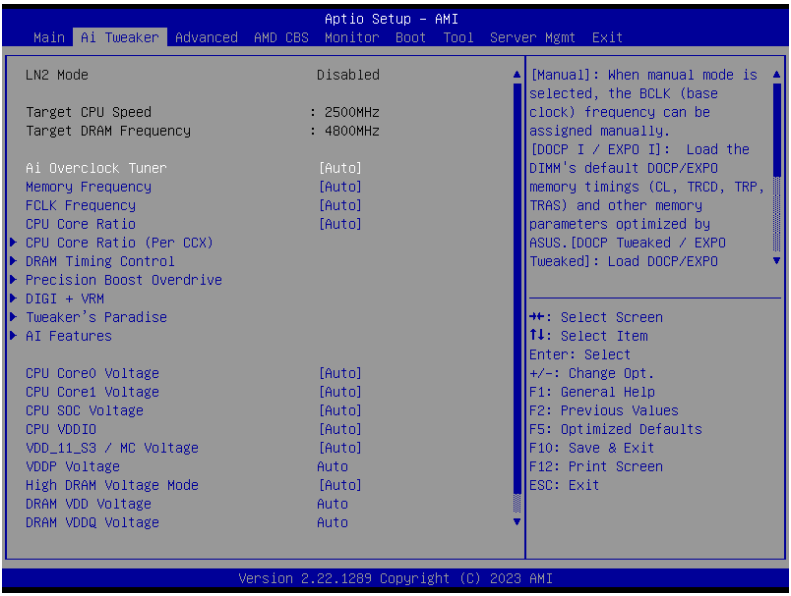
6. Ai Tweaker menu

The Ai Tweaker menu items allow you to configure overclocking-related items.

- Be cautious when changing the settings of the Ai Tweaker menu items. Incorrect field values can cause the system to malfunction.
- When overclocking, the warranty coverage declared by AMD official will be affected if you select **[Accept]** when the AMD warranty information statement appears. For more details please refer to the AMD official website.

The configuration options for this section vary depending on the CPU and DIMM model you installed on the motherboard.

Scroll down to display other BIOS items.



Ai Overclock Tuner

[Auto]	Loads the optimal settings for the system.
[Manual]	Allows you to manually assign BCLK (base clock) frequency.
[DOCP I]	Load the DIMM's default DOCP memory timings (CL, TRCD, TRP, TRAS) and other memory parameters optimized by ASUS.
[DOCP II]	Load the DIMM's complete default DOCP profile.
[DOCP Tweaked]	Load DOCP profile with tweaks for improved performance if config matches.
[EXPO I]	Load the DIMM's default EXPO memory timings (CL, TRCD, TRP, TRAS) and other memory parameters optimized by ASUS.
[EXPO II]	Load the DIMM's complete default EXPO profile.
[EXPO Tweaked]	Load EXPO profile with tweaks for improved performance if config matches.

- The configuration options for this item depends on the DIMM installed.
- The following item appears only when Ai Overclock Tuner is set to **[DOCP I]**, **[DOCP II]**, or **[DOCP Tweaked]**.

DOCP

Allows you to select your DOCP Profile. Each profile has its own DRAM frequency, timing and voltage.

The following item appears only when **Ai Overclock Tuner** is set to **[EXPO I]**, **[EXPO II]**, or **[EXPO Tweaked]**.

EXPO

Allows you to select your EXPO Profile. Each profile has its own DRAM frequency, timing and voltage.

The following items appear only when **Ai Overclock Tuner** is set to **[Manual]**, **[DOCP I]**, **[DOCP II]**, **[DOCP Tweaked]**, **[EXPO I]**, **[EXPO II]**, **[EXPO Tweaked]**, or **[AEMP]**

eCLK Mode

Configuration options: [Auto] [Synchronous mode] [Asynchronous mode]

BCLK1 Frequency

Adjusts Base Clock Frequency for DRAM, PCIE CLK. Default is 100. Use the <+> or <-> to adjust the value. The values range from 80.0000 to 1000.0000 with an interval of 0.0500. Configuration options: [Auto] [80.0000] - [1000.0000]

- Changing the BCLK will affect stability of devices, in particular SATA devices.
- The following item appears only when **eCLK Mode** is set to **[Asynchronous mode]**.

BCLK2 Frequency

BCLK2 frequency is only for CPU CLK. Use the <+> or <-> to adjust the value. The values range from 80.0000 to 1000.0000 with an interval of 0.0500.
Configuration options: [Auto] [80.0000] - [1000.0000]

PCIE Frequency

Adjusts Base Clock Frequency for G-Link. Default is 100. Use the <+> or <-> to adjust the value. The values range from 80.0000 to 200.0000 with an interval of 0.1000.
Configuration options: [Auto] [80.0000] - [200.0000]

Memory Frequency

Forces a DDR5 frequency slower than the common tCK detected via SPD.
Configuration options: [Auto] [DDR5-2000MHz] - [DDR5-12000MHz]

The configuration options for this item vary depending on the DIMM model you installed on the motherboard.

FCLK Frequency

Specifies the FCLK frequency.
Configuration options: [Auto] [800MHz] - [3000MHz]

CPU Core Ratio

Configuration options: [Auto] [CPU Core Ratio] [AI Optimized]

The following item appears only when **CPU Core Ratio** is set to **[CPU Core Ratio]**.

CPU Core Ratio

Allows you to set the CPU core ratio. Use the <+> or <-> to adjust the value. The values range from 8.00 to 100.00 with an interval of 0.25.
Configuration options: [Auto] [8.00] - [100.00]

CPU Core Ratio (Per CCX)

The sub-items in this menu allow you to adjust Core Ratios for each CCX.

Core VID 0~1

Allows you to specify a custom CPU core VID. Power saving features for idle cores (e.g. cc6 sleep) remain active.
Configuration options: [Auto] [0.700] - [1.550]

CCD 0

CCX0 Ratio (Rail0)

Allows you to specify a custom Core Ratio for this CCX. Use the <+> or <-> to adjust the value. The values range from 8.00 to 100.00 with an interval of 0.25.
Configuration options: [Auto] [8.00] - [100.00]

CCD 1

CCX0 Ratio (Rail1)

Allows you to specify a custom Core Ratio for this CCX. Use the <+> or <-> to adjust the value. The values range from 8.00 to 100.00 with an interval of 0.25.
Configuration options: [Auto] [8.00] - [100.00]

CCD 2

CCX0 Ratio (Rail1)

Allows you to specify a custom Core Ratio for this CCX. Use the <+> or <-> to adjust the value. The values range from 8.00 to 100.00 with an interval of 0.25.
Configuration options: [Auto] [8.00] - [100.00]

CCD 3

CCX0 Ratio (Rail0)

Allows you to specify a custom Core Ratio for this CCX. Use the <+> or <-> to adjust the value. The values range from 8.00 to 100.00 with an interval of 0.25.
Configuration options: [Auto] [8.00] - [100.00]

CCD 4

CCX0 Ratio (Rail0)

Allows you to specify a custom Core Ratio for this CCX. Use the <+> or <-> to adjust the value. The values range from 8.00 to 100.00 with an interval of 0.25.
Configuration options: [Auto] [8.00] - [100.00]

CCD 5

CCX0 Ratio (Rail1)

Allows you to specify a custom Core Ratio for this CCX. Use the <+> or <-> to adjust the value. The values range from 8.00 to 100.00 with an interval of 0.25.
Configuration options: [Auto] [8.00] - [100.00]

CCD 6

CCX0 Ratio (Rail1)

Allows you to specify a custom Core Ratio for this CCX. Use the <+> or <-> to adjust the value. The values range from 8.00 to 100.00 with an interval of 0.25.
Configuration options: [Auto] [8.00] - [100.00]

CCD 7

CCX0 Ratio (Rail0)

Allows you to specify a custom Core Ratio for this CCX. Use the <+> or <-> to adjust the value. The values range from 8.00 to 100.00 with an interval of 0.25.
Configuration options: [Auto] [8.00] - [100.00]

CCD 8

CCX0 Ratio (Rail0)

Allows you to specify a custom Core Ratio for this CCX. Use the <+> or <-> to adjust the value. The values range from 8.00 to 100.00 with an interval of 0.25.
Configuration options: [Auto] [8.00] - [100.00]

CCD 9

CCX0 Ratio (Rail1)

Allows you to specify a custom Core Ratio for this CCX. Use the <+> or <-> to adjust the value. The values range from 8.00 to 100.00 with an interval of 0.25.
Configuration options: [Auto] [8.00] - [100.00]

CCD 10

CCX0 Ratio (Rail1)

Allows you to specify a custom Core Ratio for this CCX. Use the <+> or <-> to adjust the value. The values range from 8.00 to 100.00 with an interval of 0.25.
Configuration options: [Auto] [8.00] - [100.00]

CCD 11

CCX0 Ratio (Rail0)

Allows you to specify a custom Core Ratio for this CCX. Use the <+> or <-> to adjust the value. The values range from 8.00 to 100.00 with an interval of 0.25.
Configuration options: [Auto] [8.00] - [100.00]

Dynamic OC Switcher

Enabling this dynamically switches back and forth between OC mode and Default modes based on current and temperature threshold specified.
Configuration options: [Auto] [Disabled] [Enabled]

The following items appear only when **Dynamic OC Switcher** is set to **[Enabled]**.

Current Threshold to Switch to OC Mode

Set this threshold to control when the CPU goes into OC Mode and when it comes back to default. Bigger than this value = OC Mode, smaller than this value = Default Mode. We recommend a value of 40A for single CCD and 60A for two CCDs. Leave Auto for board to decide optimal value.
Configuration options: [Auto] [0] - [65535]

Calibrated Temperature Threshold to switch back

Set this threshold to control when the CPU returns to default mode. When CPU Calibrated Temperature is bigger than this threshold, CPU returns to default. Likewise, when temperature is smaller than this threshold AND current is bigger than Current Threshold, CPU slips into OC Mode. In Celsius Unit.
Configuration options: [Auto] [0] - [140]

Hysteresis

Higher number increase the time required to persist in state when crossing thresholds before switching. Set 0 for fastest reaction and increase this to require longer times to remain said state before activation.
Configuration options: [Auto] [0] - [255]

DRAM Timing Control

The sub-items in this menu allow you to set the DRAM timing control features. Use the <+> and <-> keys to adjust the value. To restore the default setting, type **[Auto]** using the keyboard and press the <Enter> key. You can also select various **Memory Presets** to load settings suitably tuned for some memory modules.

Changing the values in this menu may cause the system to become unstable! If this happens, revert to the default settings.

Primary Timings

Primary Timings Report

Allows you to view the Primary Timings Report.

Tcl

DRAM CAS# Latency, the value stepping is 2.
Configuration options: [Auto] [2] - [64]

Trcd

DRAM RAS# to CAS# Delay.
Configuration options: [Auto] [1] - [63]

Trp

DRAM RAS# PRE Time.
Configuration options: [Auto] [1] - [63]

Tras

DRAM RAS# ACT Time.
Configuration options: [Auto] [1] - [127]

Secondary Timings

Secondary Timings Report

Allows you to view the Secondary Timings Report.

Trc

DRAM Row Cycle Time.
Configuration options: [Auto] [1] - [255]

Twr

DRAM WRITE to READ Delay, the value stepping is 6.
Configuration options: [Auto] [48] - [126]

Refresh Interval

Configuration options: [Auto] [1] - [65535]

Trfc1

DRAM REF Cycle Time.
Configuration options: [Auto] [1] - [4095]

Trfc2

Configuration options: [Auto] [1] - [4095]

Trfcsb

Configuration options: [Auto] [1] - [2047]

Trtp

DRAM READ to PRE Time.
Configuration options: [Auto] [1] - [31]

TrrdL

DRAM RAS# to RAS# Delay(tRRDL).
Configuration options: [Auto] [1] - [31]

TrrdS

DRAM RAS# to RAS# Delay(tRRDS).
Configuration options: [Auto] [1] - [31]

Tfaw

Configuration options: [Auto] [1] - [127]

TwtrL

DRAM WRITE to READ Delay(tWTR_L).
Configuration options: [Auto] [1] - [127]

TwtrS

DRAM WRITE to READ Delay(tWTR_S).
Configuration options: [Auto] [1] - [31]

TrdrdScl

Configuration options: [Auto] [1] - [15]

TrdrdSc

Configuration options: [Auto] [1] - [15]

TrdrdSd

Configuration options: [Auto] [1] - [15]

Trdrddd

Configuration options: [Auto] [1] - [15]

TwrwrScl

Configuration options: [Auto] [1] - [63]

TwrwrSc

Configuration options: [Auto] [1] - [15]

TwrwrSd

Configuration options: [Auto] [1] - [15]

TwrwrDd

Configuration options: [Auto] [1] - [15]

Twrrd

Configuration options: [Auto] [1] - [15]

Trdwr

Configuration options: [Auto] [1] - [63]

Additional Timings

IBUF_LPWR_MODE

Configuration options: [Auto] [Enabled] [Disabled]

ADDR_CMD_MODE

Configuration options: [Auto] [Buf] [UnBuf]

M_ORDERING

Configuration options: [Auto] [NORM] [STRICT] [RELAXED]

S_COL_WIDTH

Configuration options: [Auto] [0] - [15]

MC_SVA_TRIM0

Configuration options: [Auto] [0] - [255]

MC_SVA_TRIM1

Configuration options: [Auto] [0] - [255]

MC_SVA_TRIM2

Configuration options: [Auto] [0] - [255]

MMCM_MULT_F

Configuration options: [Auto] [Enabled] [Disabled]

Sub Urgent Refresh Lower Bound

Configuration options: [Auto] [1] - [6]

Urgent Refresh Limit

Specifies the stored refresh limit required to enter urgent refresh mode. Constraint: SubUrgRefLowerBound <= UrgRefLimit Valid value: 6~1.
Configuration options: [Auto] [1] - [6]

DRAM Refresh Rate

DRAM refresh rate: 1.95us or 3.9us (default).
Configuration options: [3.9 usec] [1.95 usec]

Self-Refresh Exit Staggering

Tcksrx += (Trfc/n * (UMC_NUMBER % 3)) Selectable by CBS Option: Disable Staggering n = 1 <= Stagger Channels by ~270 ns, n=2 n=3 n=4... n=9 <= Stagger Channels By ~30 ns (Default).
Configuration options: [Auto] [Disabled] [n = 1] [n = 2] [n = 3] [n = 4] [n = 5] [n = 6] [n = 7] [n = 8] [n = 9]

DRAM Signal Control

Proc CA Drive Strength

Configuration options: [Auto] [120 ohm] [60 ohm] [40 ohm] [30 ohm]

Proc Data Drive Strength

Configuration options: [Auto] [120 ohm] [60 ohm] [40 ohm] [30 ohm]

Proc Data Drive Strength

Configuration options: [Auto] [High Impedance] [240 ohm] [120 ohm] [80 ohm] [60 ohm] [48 ohm] [40 ohm] [34.3 ohm]

CPU On-Die Termination

CPU On-Die Termination(ProcODT)
Configuration options: [Auto] [High Impedance] [480 ohm] [240 ohm] [160 ohm] [120 ohm] [96 ohm] [80 ohm] [68.6 ohm] [60 ohm] [53.3 ohm] [48 ohm] [43.6 ohm] [40 ohm] [36.9 ohm] [34.3 ohm] [32 ohm] [30 ohm] [28.2 ohm] [26.7 ohm] [25.3 ohm]

DRAM Data Drive Strength

Configuration options: [Auto] [48 ohm] [40 ohm] [34 ohm]

Rtt Nom Wr

Configuration options: [Auto] [RTT_OFF] [RZQ (240)] [RZQ/2 (120)] [RZQ/3 (80)] [RZQ/4 (60)] [RZQ/5 (48)] [RZQ/6 (40)] [RZQ/7 (34)]

Rtt Nom Rd

Configuration options: [Auto] [RTT_OFF] [RZQ (240)] [RZQ/2 (120)] [RZQ/3 (80)] [RZQ/4 (60)] [RZQ/5 (48)] [RZQ/6 (40)] [RZQ/7 (34)]

Rtt Wr

Configuration options: [Auto] [RTT_OFF] [RZQ (240)] [RZQ/2 (120)] [RZQ/3 (80)] [RZQ/4 (60)] [RZQ/5 (48)] [RZQ/6 (40)] [RZQ/7 (34)]

Rtt Park

Configuration options: [Auto] [RTT_OFF] [RZQ (240)] [RZQ/2 (120)] [RZQ/3 (80)] [RZQ/4 (60)] [RZQ/6 (40)] [RZQ/7 (34)]

Rtt Park Dqs

Configuration options: [Auto] [RTT_OFF] [RZQ (240)] [RZQ/2 (120)] [RZQ/3 (80)] [RZQ/4 (60)] [RZQ/5 (48)] [RZQ/6 (40)] [RZQ/7 (34)]

Power Down Enable

Configuration options: [Disabled] [Enabled] [Auto]

Memory Context Restore

Configure the memory context restore mode. When enabled, DRAM re-retraining is avoided when possible and the POST latency is minimized.
Configuration options: [Auto] [Enabled] [Disabled]

UCLK DIV1 MODE

Configuration options: [Auto] [UCLK=MEMCLK] [UCLK=MEMCLK/2]

CA Tx Phase Shift Clk

Configuration options: [Auto] [0] - [7]

CS Tx Phase Shift Clk

Configuration options: [Auto] [0] - [7]

CK Tx Phase Shift Clk

Configuration options: [Auto] [0] - [7]

CA Rx Phase Shift Clk

Configuration options: [Auto] [0] - [7]

CS Rx Phase Shift Clk

Configuration options: [Auto] [0] - [7]

CK Rx Phase Shift Clk

Configuration options: [Auto] [0] - [7]

FIFO Wr En Fine Delay

Configuration options: [Auto] [0] - [1]

POC Sample PD

Configuration options: [Auto] [Enabled] [Disabled]

Bank Swap Mode

Configuration options: [Auto] [Disabled] [Swap CPU] [Swap APU]

Mem Over Clock Fail Count

Configuration options: [Auto] [RTT_OFF] [RZQ (240)] [RZQ/2 (120)] [RZQ/3 (80)] [RZQ/4 (60)] [RZQ/5 (48)] [RZQ/6 (40)] [RZQ/7 (34)]

Additional Memory Tweaks

DDR Training Runtime Reduction

[Disabled]	Force Disable DDR Training Runtime Reduction.
[Enabled]	Force Enable DDR Training Runtime Reduction.
[Auto]	Default code behavior. If OC is ENABLE, DDR Training Runtime Reduction will be DISABLE by DEFAULT.

DDR5 Nitro Mode

Can improve overclocked memory support for modules over 6000Mt/s with potential boot time and/or latency tradeoffs.
Configuration options: [Auto] [Enabled] [Disabled]

The following items appear only when **DDR5 Nitro Mode** is set to **[Enabled]**.

DDR5 Robust Training Mode

A more comprehensive memory training algorithm that increases boot time but can result in improved stability at overclocked memory settings.
Configuration options: [Auto] [Enabled] [Disabled]

Nitro RX Data

Configures the RX Timing between memory controller and PHY. Higher value may enable increased memory frequency at the expense of increased latency.
Configuration options: [Auto] [1] [2] [Disabled]

Nitro TX Data

Configures the TX Timing between memory controller and PHY. Higher value may enable increased memory frequency at the expense of increased latency.
Configuration options: [Auto] [0] [1] [2] [3] [Disabled]

Nitro Control Line

Configures the command timing latency between the memory controller and PHY. Higher value may enable increased memory frequency at the expense of increased latency.
Configuration options: [Auto] [0] [1] [Disabled]

Nitro RX Burst Length

DQ Training Pattern Length - Higher number results in more robust training and longer runtime. Lower number results in less robust training and shorter runtime, but potentially less stability.
Configuration options: [Auto] [1x] [2x] [4x] [8x]

Nitro TX Burst Length

DQ Training Pattern Length - Higher number results in more robust training and longer runtime. Lower number results in less robust training and shorter runtime, but potentially less stability.
Configuration options: [Auto] [1x] [2x] [4x] [8x]

TX DFE Taps

Specifies the number of TX DFE taps.
Configuration options: [Auto] [1] - [4]

RX DFE Taps

Specifies the number of RX DFE taps.
Configuration options: [Auto] [1] - [4]

RX2D_TrainOpt

Configuration options: [Auto] [Manual]

The following items appear only when **RX2D_TrainOpt** is set to **[Manual]**.

RX2D_DFE

Used to force Rx DFE on or off.
Configuration options: [Auto] [Disabled] [Enabled]

RX2D Voltage Step Size (2^n)

0 = 1 DAC setting between checked values. 1 = 2 DAC settings between checked values. 2 = 4 DAC settings between checked values. 3 = 8 DAC settings between checked values.
Configuration options: [Auto] [1 DAC steps per loop] [2 DAC steps per loop] [4 DAC steps per loop] [8 DAC steps per loop]

RX2D Delay Step Size (2^n)

0 = 1 LCDL delays between checked values. 1 = 2 LCDL delays between checked values. 2 = 4 LCDL delays between checked values. 3 = 8 LCDL delays between checked values.
Configuration options: [Auto] [1 DAC steps per loop] [2 DAC steps per loop] [4 DAC steps per loop] [8 DAC steps per loop]

TX2D_TrainOpt

Configuration options: [Auto] [Manual]

The following items appear only when **TX2D_TrainOpt** is set to **[Manual]**.

TX2D_DFE

Configuration options: [Auto] [Disabled] [Enabled]

TX2D Voltage Step Size (2^n)

0 = 1 DAC setting between checked values. 1 = 2 DAC settings between checked values. 2 = 4 DAC settings between checked values. 3 = 8 DAC settings between checked values.
Configuration options: [Auto] [1 DAC steps per loop] [2 DAC steps per loop] [4 DAC steps per loop] [8 DAC steps per loop]

TX2D Delay Step Size (2^n)

0 = 1 LCDL delays between checked values. 1 = 2 LCDL delays between checked values. 2 = 4 LCDL delays between checked values. 3 = 8 LCDL delays between checked values.
Configuration options: [Auto] [1 DAC steps per loop] [2 DAC steps per loop] [4 DAC steps per loop] [8 DAC steps per loop]

TX2D Voltage Step Multiplier

0 = Voltage Step Size is not modified. 1 = Voltage Step Size is multiplied by 16.
Configuration options: [Auto] [Multiply DAC step size by 16] [No Multiply]

TX2D Delay Step Multiplier

0 = Delay Step Size is not modified. 1 = Delay Step Size is multiplied by 16.
Configuration options: [Auto] [Multiply DAC step size by 16] [No Multiply]

Precision Boost Overdrive

Medium Load Boostit

Enabling may help improve performance under medium loads.
Configuration options: [Auto] [Disabled] [Enabled]

Precision Boost Overdrive

When this item is enabled, it allows the processor to run beyond defined values for PPT, VDD_CPU EDC, VDD_CPU TDC, VDD_SOC EDC, VDD_SOC TDC to the limits of the board, and allows it to boost at higher voltages for longer durations than default operation.
Configuration options: [Auto] [Disabled] [Enabled] [Manual] [Enhancement]

The following items appear only when **Precision Boost Overdrive** is set to **[Manual]**.

PPT Limit

PPT Limit [W], Board Socket Power capability, adjustable up to motherboard's programmed PPT limit.
Configuration options: [Auto] [0] - [65535]

TDC Limit

TDC Limit [A], Board thermally constrained current delivery capacity, adjustable up to motherboard's programmed board TDC limit.
Configuration options: [Auto] [0] - [65535]

EDC Limit

EDC Limit [A], Board electrically constrained current delivery capacity, adjustable up to motherboard's programmed board EDC limit.
Configuration options: [Auto] [0] - [65535]

The following item appears only when **Precision Boost Overdrive** is set to **[Enhancement]**.

Thermal Limit

Configuration options: [Level 1 (90°C)] [Level 2 (80°C)] [Level 3 (70°C)]

Precision Boost Overdrive Scalar

[Auto]	Part runs with a scalar of 1X, i.e. normal operation.
[Manual]	Part runs with a scalar of customized value.

The following item appears only when **Precision Boost Overdrive Scalar** is set to **[Manual]**.

Customized Precision Boost Overdrive Scalar

Precision Boost Overdrive increases the maximum boost voltage used (runs above parts specified maximum) and the amount of time spent at that voltage. The larger the value entered the larger the boost voltage used and the longer that voltage will be maintained.
Configuration options: [1X] - [10X]

CPU Boost Clock Override

Allows you to increase (positive) or decrease (negative) the maximum CPU frequency that may be automatically achieved by the CPU Boost Algorithm.
Configuration options: [Auto] [Disabled] [Enabled (Positive)] [Enabled (Negative)]

The following item appears only when **CPU Boost Clock Override** is set to **[Enabled (Positive)]**.

Max CPU Boost Clock Override(+)

Increases the maximum CPU frequency that may be automatically achieved by the Precision Boost 2 algorithm.
Configuration options: [Auto] [0] - [200]

The following item appears only when **CPU Boost Clock Override** is set to **[Enabled (Negative)]**.

Max CPU Boost Clock Override(-)

Decreases the maximum CPU frequency that may be automatically achieved by the Precision Boost 2 algorithm.
Configuration options: [Auto] [0] - [200]

Per-Core Boost Clock Limit

Per-Core Boost Clock Limit

Set specific limits to each core in MHz unit. This will still be capped by the global CPU Boost clock but limiting down from this for each core will restrain its frequency. Limiting a weaker core may improve its curve optimizer margin.
Configuration options: [Auto] [Disabled] [Enabled]

The following items appear only when **Per-Core Boost Clock Limit** is set to **[Enabled]**.

Core 0~95

The recommended value is based on parameters of your setup with the current settings of Ai Tweaker menu.
Configuration options: [Auto] [3600] - [7000]

Platform Thermal Throttle Limit

Allows you to decrease the maximum allowed processor temperature (celsius).
Configuration options: [Auto] [Manual]

The following item appears only when **Platform Thermal Throttle Limit** is set to **[Manual]**.

Platform Thermal Throttle Limit

Configuration options: [0] - [255]

Curve Optimizer

Curve Optimizer

Allows the user to shift the Voltage / Frequency (AVFS) curve to include higher voltages (positive values) or lower voltages (negative values). The larger the value entered the larger the magnitude of the voltage shift.
Configuration options: [Auto] [All Cores] [Per Core]

The following items appear only when **Curve Optimizer** is set to **[All Cores]**.

All Core Curve Optimizer Sign

Determines the direction of the curve shift on all cores. Positive shifts the curve up to use higher voltages. Negative shifts the curve down to use lower voltages.
Configuration options: [Positive] [Negative]

All Core Curve Optimizer Magnitude

Determines the magnitude of the curve shift to be made (entered in whole numbers) the larger the value entered the larger the magnitude of the shift.
Configuration options: [0] - [60]

The following items appear only when **Curve Optimizer** is set to **[Per Core]**.

Core 0~95 Curve Optimizer Sign

Determines the direction of the curve shift on this core. Positive shifts the curve up to use higher voltages. Negative shifts the curve down to use lower voltages.
Configuration options: [Positive] [Negative]

Core 0~95 Curve Optimizer Magnitude

Determines the magnitude of the curve shift to be made to this core (entered in whole numbers) the larger the value entered the larger the magnitude of the shift.
Configuration options: [0] - [30]

Digi+ VRM

VRM Initialization Check

When any error occurs during VRM initialization, the system will hang at POST code 77 if this function is enabled.
Configuration options: [Disabled] [Enabled]

CPU Rail0~1 Load-line Calibration

CPU Load-Line Calibration is defined by AMD VRM spec and affects CPU voltage. The CPU working voltage will decrease proportionally to CPU loading. Higher value could get higher voltage and good overclocking performance but increase the CPU and VRM thermal.
Configuration options [Auto] [Level 1] [Level 2] [Level 3] [Level 4] [Level 5] [Level 6] [Level 7] [Level 8]

DO NOT remove the thermal module. The thermal conditions should be monitored.

Segment 2 Loadline

Segment 2 Loadline implements a customized Loadline for high CPU Workloads whose boundary is defined by Segment 2 Current Threshold. This can be a different value from CPU Loadline Calibration for finer control. Lower values result in a higher voltage droop.
Configuration options: [Disabled] [Level 1] [Level 2] [Level 3] [Level 4] [Level 5] [Level 6] [Level 7]

The following item appears only when **Segment 2 Loadline** is set to **[Level 1]**, **[Level 2]**, **[Level 3]**, **[Level 4]**, **[Level 5]**, **[Level 6]**, or **[Level 7]**.

Segment2 Current Threshold

Segment 2 Current Threshold sets the boundary between CPU Loadline Calibration and Segment 2 Loadline. Unit is in amps. When current is lower than threshold, VRM loadline follows CPU Loadline Calibration value. When current is higher threshold, VRM loadline follows Segment2 Loadline value.
Configuration options: [1] - [1023]

CPU Rail0~1 Current Reporting Scale

The scale for the current reported to the CPU via the SVI bus.
Configuration options [Auto] [100%] [75%] [50%] [25%]

CPU Rail0~1 VRM Switching Frequency

Sets the VRM switching frequency. VRM switching frequency affects transient response and VRM component temperatures. Setting a higher switching frequency will result in better transient response at the expense of higher VRM temperatures. Active cooling of the VRM heatsink is recommended when running high CPU voltage and high load-line calibration values.
Configuration options: [Auto] [Manual]

DO NOT remove the thermal module. The thermal conditions should be monitored.

The following item appears only when **CPU Rail0~1 VRM Switching Frequency** is set to **[Auto]**.

VRM Spread Spectrum

Reduce the margin of peak noise from VRM. Enable to reduce peak noise. Disable this setting when overclocking.
Configuration options: [Disabled] [Enabled]

The following item appears only when **CPU Rail0~1 VRM Switching Frequency** is set to **[Manual]**.

Fixed CPU Rail0~1 VRM Switching Frequency(KHz)

The switching frequency will affect the VRM transient response speed and the component thermal production. Configure a higher frequency to get a quicker transient response speed. The values range from 300 KHz to 1000 KHz with an interval of 50 KHz.

CPU Rail0~1 Power Duty Control

CPU power duty control adjusts the current and thermal of every VRM phase component.

[T. Probe]	Select to maintain VRM thermal balance.
[Extreme]	Select to maintain VRM current balance.

DO NOT remove the thermal module when setting this item to **[Extreme]**. The thermal conditions should be monitored.

CPU Rail0~1 Power Phase Control

Allows you to set the power phase control of the CPU.

[Auto]	Automatically selects the power phase control.
[Standard]	The number of active phases is controlled by the CPU.
[Extreme]	Sets full phase mode.
[Manual]	Manually select the power phase response speed.

DO NOT remove the thermal module when setting this item to **[Extreme]**. The thermal conditions should be monitored.

The following item appears only when **CPU Rail0~1 Power Phase Control** is set to **[Manual]**.

Power Phase Response

Select ultra fast mode for a faster power phase response. The reaction time will be longer when regular mode is selected.
Configuration options: [Ultra Fast] [Fast] [Medium] [Regular]

CPU Power Thermal Control

A higher temperature brings a wider CPU power thermal range and extends the overclocking tolerance to enlarge O.C. potential.
Configuration options: [Auto] [125] - [135]

DO NOT remove the thermal module. The thermal conditions should be monitored.

Core Voltage Suspension

Manipulates voltage output, effective in both over-ride and non over-ride modes.
Configuration options: [Auto] [Disabled] [Enabled]

The following items appear only when **Core Voltage Suspension** is set to **[Enabled]**.

Voltage Floor Mode

[Static]	Sets a fixed minimum voltage.
[Dynamic]	Sets a customized minimum that actively moves based on CPU temperature.

The following item appears only when **Voltage Floor Mode** is set to **[Static]**.

Voltage Floor

Boosts output to keep voltage above this level, efficacy up to 0.3V. Use the <+> and <-> keys to adjust the value. The values range from 0.000V to 1.700V with an interval of 0.00625V.
Configuration options: [Auto] [0.00000] - [1.70000]

The following items appear only when **Voltage Floor Mode** is set to **[Dynamic]**.

Floor Low VMin

The lowest minimum voltage point that maps to Floor Hot Temp should the processor temperature move to hotter or equal to Floor Hot Temp. Auto is 1.05V. Use the <+> and <-> keys to adjust the value. The values range from 0.000V to 1.700V with an interval of 0.00625V.
Configuration options: [Auto] [0.00000] - [1.70000]

Floor Hot Temp

The hottest temperature point that maps to Floor Low Vmin should the processor temperature move to hotter or equal to Floor Hot Temp. Auto is 95C. Use the <+> and <-> keys to adjust the value. The values range from 0C to 255C with an interval of 1C.
Configuration options: [Auto] [0] - [255]

Floor High VMin

The highest minimum voltage point that maps to Floor Cold Temp should the processor temperature move to colder or equal to Floor Cold Temp. Auto is 1.30V. Use the <+> and <-> keys to adjust the value. The values range from 0.000V to 1.700V with an interval of 0.00625V.
Configuration options: [Auto] [0.00000] - [1.70000]

Floor Cold Temp

The coldest temperature point that maps to Floor High Vmin should the processor temperature move to colder or equal to Floor Cold Temp. Auto is 55C. Use the <+> and <-> keys to adjust the value. The values range from 0C to 255C with an interval of 1C.
Configuration options: [Auto] [0] - [255]

Voltage Ceiling Mode

[Static]	Sets a fixed maximum voltage.
[Dynamic]	Sets a customized maximum that actively moves based on CPU temperature.

The following item appears only when **Voltage Ceiling Mode** is set to **[Static]**.

Voltage Ceiling

Suppresses output to keep voltage below this level, efficacy up to 0.3V. Use the <+> and <-> keys to adjust the value. The values range from 0.000V to 1.700V with an interval of 0.00625V.
Configuration options: [Auto] [0.00000] - [1.70000]

The following items appear only when **Voltage Ceiling Mode** is set to **[Dynamic]**.

Ceiling Low VMax

The lowest maximum voltage point that maps to Ceiling Hot Temp should the processor temperature move to hotter or equal to Ceiling Hot Temp. Auto is 1.20V. Use the <+> and <-> keys to adjust the value. The values range from 0.000V to 1.700V with an interval of 0.00625V.
Configuration options: [Auto] [0.00000] - [1.70000]

Ceiling Hot Temp

The hottest temperature point that maps to Ceiling Low VMax should the processor temperature move to hotter or equal to Ceiling Hot Temp. Auto is 88C. Use the <+> and <-> keys to adjust the value. The values range from 0C to 255C with an interval of 1C.
Configuration options: [Auto] [0] - [255]

Ceiling High VMax

The highest maximum voltage point that maps to Ceiling Cold Temp should the processor temperature move to colder or equal to Ceiling Cold Temp. Auto is 1.45V. Use the <+> and <-> keys to adjust the value. The values range from 0.000V to 1.700V with an interval of 0.00625V.
Configuration options: [Auto] [0.00000] - [1.70000]

Ceiling Cold Temp

The coldest temperature point that maps to Ceiling High VMax should the processor temperature move to colder or equal to Ceiling Cold Temp. Auto is 65C. Use the <+> and <-> keys to adjust the value. The values range from 0C to 255C with an interval of 1C.
Configuration options: [Auto] [0] - [255]

VDDSOC Switching Frequency

Configuration options: [Auto] [Manual]

The following item appears only when **VDDSOC Switching Frequency** is set to **[Manual]**.

Fixed VDDSOC VRM Switching Frequency(KHz)

Allows you to set a higher frequency for a quicker transient response speed. The values range from 400 KHz to 700 KHz with an interval of 100 KHz.

VDDSOC Power Phase Control

Configuration options: [Auto] [Standard] [Extreme] [Manual]

DO NOT remove the thermal module when setting this item to **[Extreme]**. The thermal conditions should be monitored.

The following item appears only when **VDDSOC Power Phase Control** is set to **[Manual]**.

Power Phase Response

Select ultra fast mode for a faster power phase response. The reaction time will be longer when regular mode is selected.
Configuration options: [Ultra Fast] [Fast] [Medium] [Regular]

VDDIO Switching Frequency

Configuration options: [Auto] [Manual]

The following item appears only when **VDDIO Switching Frequency** is set to **[Manual]**.

Fixed VDDIO VRM Switching Frequency(KHz)

Allows you to set a higher frequency for a quicker transient response speed. The values range from 400 KHz to 700 KHz with an interval of 100 KHz.

VDDIO Power Phase Control

Configuration options: [Auto] [Standard] [Extreme] [Manual]

DO NOT remove the thermal module when setting this item to **[Extreme]**. The thermal conditions should be monitored.

The following item appears only when **VDDIO Power Phase Control** is set to **[Manual]**.

Power Phase Response

Select ultra fast mode for a faster power phase response. The reaction time will be longer when regular mode is selected.
Configuration options: [Ultra Fast] [Fast] [Medium] [Regular]

DRAM Switching Frequency

This item allows you to set the VRM switching frequency. VRM switching frequency affects transient response and VRM component temperatures. Setting a higher frequency will result in better transient response at the expense of more switching noise.
Configuration options: [Auto] [Manual]

The following item appears only when **DRAM Switching Frequency** is set to **[Manual]**.

Fixed DRAM Switching Frequency (KHz)

The DRAM switching frequency will affect the overclocking range and the system stability. Configure a higher frequency to increase the overclocking range or a lower frequency to enhance the system stability. Use the <+> or <-> to adjust the value. The values range from 500kHz to 800kHz with an interval of 100kHz.

DRAM Power Phase Control

Configuration options: [Auto] [Standard] [Extreme]

Tweaker's Paradise

Clock Spread Spectrum

Allows you to enable or disable Clock Spread Spectrum.
Configuration options: [Auto] [Enabled] [Disabled]

BCLK1 Amplitude

Allows you to set the signal magnitude of the reference BCLK1 supplied to the processor. Higher values may improve overclocking stability.
Configuration options: [Auto] [800mV] [900mV]

BCLK1 Slew Rate

The speed at which the base clock rises or falls. Set a high value for overclocking stability.
Configuration options: [Auto] [Slow] [High]

Chipset1_1.0V

Use the <+> and <-> keys to adjust the value. The values range from 0.800V to 1.400V with an interval of 0.005V.
Configuration options: [Auto] [0.80000] - [1.40000]

1.8V_RUN

Use the <+> or <-> to adjust the value. The values range from 1.500V to 2.500V with an interval of 0.010V.
Configuration options: [Auto] [1.50000] - [2.50000]

Sense MI Skew 1~4

Configuration options: [Auto] [Disabled] [Enabled]

Sense MI Skew 1~4

Configuration options: [Auto] [0] - [127]

Raise RComp

Configuration options: [Auto] [Disabled] [Enabled]

AI Features

The items in this menu allows you to enable or disable different AI Features.

Cooler Efficiency Customize

[Keep Training]	Continuous evaluations will be performed on Cooler efficiency and updated accordingly.
[Stop Training]	Cooler efficiency evaluations will stop and current evaluated efficiency will be used.
[User Specify]	Manually specify the Cooler efficiency and all predictions will be based off this manual setting.

The following item appears only when **Cooler Efficiency Customize** is set to **[User Specify]**.

Cooler Score

The value of the Cooler's pts. [Maximum] 250 pts; [Minimum] 1 pts; [Default] 125 pts.
Configuration options: [1] - [250]

Recalibrate Cooler

Allows you to recalibrate your cooler efficiency.

Cooler Re-evaluation Algorithm

Allows you to set how inclined the re-evaluation will update.
Configuration options: [Normal] [More inclined to update] [Very inclined to update] [Less inclined to update] [Least inclined to update]

Optimism Scale

Allows you to set the optimism of the predictions. The higher the value, the more optimistic the predictions and vice versa.
Configuration options: [50] - [150]

CPU Core0~1 Voltage

Allows you to increase to help CPU Core Frequency overclock. The reading shown on the right is the Core Voltage Reading from the remote ADC Sensing. The reading shown below is the true Core Voltage sensed from the processor's sensor.
Configuration options: [Auto] [Manual Mode] [Offset Mode]

The following item appears only when **CPU Core0~1 Voltage** is set to **[Manual Mode]**.

CPU Core0~1 Voltage Override

Allows you to configure the input voltage for the CPU by the external voltage regulator. Use the <+> and <-> keys to adjust the value. The values range from 0.625V to 1.500V with an interval of 0.005V.
Configuration options: [Auto] [0.62500] - [1.50000]

The following items appear only when **CPU Core0~1 Voltage** is set to **[Offset Mode]**.

Offset Mode Sign

[+] To offset the CPU core voltage by a positive value.
[–] To offset the CPU core voltage by a negative value.

CPU Core0~1 Voltage Offset

Allows you to configure the input voltage for the CPU by the external voltage regulator. Use the <+> or <-> to adjust the value. The values range from 0.005V to 0.635V with an interval of 0.005V.
Configuration options: [Auto] [0.00500] - [0.63500]

CPU SOC Voltage

Allows you to increase to help Memory Frequency overclock. The reading shown on the right is the SOC Voltage Reading from the remote ADC Sensing. The reading shown below is the true SOC Voltage sensed from the processor's sensor.
Configuration options: [Auto] [Manual Mode] [Offset Mode]

The following item appears only when **CPU SOC Voltage** is set to **[Manual Mode]**.

VDDSOC Voltage Override

Use the <+> and <-> keys to adjust the value. The values range from 0.625V to 1.300V with an interval of 0.005V.
Configuration options: [Auto] [0.62500] - [1.30000]

The following items appear only when **CPU SOC Voltage** is set to **[Offset Mode]**.

VDDSOC Offset Mode Sign

[+] To offset the CPU SOC voltage by a positive value.
[–] To offset the CPU SOC voltage by a negative value.

VDDSOC Voltage Offset

Use the <+> or <-> to adjust the value. The values range from 0.005V to 0.635V with an interval of 0.005V.
Configuration options: [Auto] [0.00500] - [0.63500]

CPU VDDIO

Configuration options: [Auto] [Manual Mode] [Offset Mode]

The following item appears only when **CPU VDDIO** is set to **[Manual Mode]**.

VDDIO Override

Use the <+> and <-> keys to adjust the value. The values range from 0.600V to 1.500V with an interval of 0.005V.
Configuration options: [Auto] [0.60000] - [1.50000]

The following items appear only when **CPU VDDIO** is set to **[Offset Mode]**.

VDDIO Offset Mode Sign

[+] To offset the CPU VDDIO by a positive value.
[–] To offset the CPU VDDIO by a negative value.

VDDIO Offset

Allows you to configure the input voltage for the CPU by the external voltage regulator. Use the <+> or <-> to adjust the value. The values range from 0.005V to 0.635V with an interval of 0.005V.
Configuration options: [Auto] [0.00500] - [0.63500]

VDD_11_S3 / MC Voltage

Configuration options: [Auto] [Manual Mode]

The following item appears only when **VDD_11_S3 / MC Voltage** is set to **[Manual Mode]**.

VDD_11_S3 Override

Use the <+> and <-> keys to adjust the value. The values range from 0.6240V to 1.7004V with an interval of 0.0039V.
Configuration options: [Auto] [0.62400] - [1.70040]

VDDP Voltage

Use the <+> or <-> to adjust the value. The values range from 0.700V to 1.800V with an interval of 0.001V.
Configuration options: [Auto] [0.70000] - [1.80000]

High DRAM Voltage Mode

If disabled, the upper range for DRAM Voltage will be 1.435V. If enabled, the upper range will be 2.070V. If enabled on non-supported DRAM, the voltage will be lower than requested.
Configuration options: [Auto] [Disabled] [Enabled]

DRAM VDD Voltage

Allows you to set the power for the DRAM IC's VDD portion. Use the <+> or <-> to adjust the value. The values range from 0.800V to 1.435V with an interval of 0.005V.
Configuration options: [Auto] [0.80000] - [1.43500]

DRAM VDDQ Voltage

Allows you to set the power for the DRAM IC's VDD Data portion. Use the <+> or <-> to adjust the value. The values range from 0.800V to 1.435V with an interval of 0.005V.
Configuration options: [Auto] [0.80000] - [1.43500]

Advanced Memory Voltages

PMIC Voltages

Configuration options: [Auto] [Sync All PMICs] [By per PMIC]

The following items appear only when **PMIC Voltages** is set to **[Sync All PMICs]**.

SPD HUB VLDO (1.8V)

Allows you to set the main power for the SPD Hub Logic. Default set to 1.8V. Use the <+> or <-> to adjust the value. The values range from 1.700V to 2.000V with an interval of 0.100V.
Configuration options: [Auto] [1.70000] - [2.00000]

SPD HUB VDDIO (1.0V)

Allows you to set the main power for the SPD Hub side-band interface. Default set to 1.0V. Use the <+> or <-> to adjust the value. The values range from 0.900V to 1.200V with an interval of 0.100V.
Configuration options: [Auto] [0.90000] - [1.20000]

Memory VDD Voltage

Allows you to set the power for the DRAM IC's VDD portion. Use the <+> or <-> to adjust the value. The values range from 0.800V to 1.435V with an interval of 0.005V.
Configuration options: [Auto] [0.80000] - [1.43500]

Memory VDDQ Voltage

Allows you to set the power for the DRAM IC's Data portion. Use the <+> or <-> to adjust the value. The values range from 0.800V to 1.435V with an interval of 0.005V.
Configuration options: [Auto] [0.80000] - [1.43500]

Memory VPP Voltage

Allows you to set the power for the DRAM Activating Power Supply. Use the <+> or <-> to adjust the value. The values range from 1.500V to 2.135V with an interval of 0.005V.
Configuration options: [Auto] [1.50000] - [2.13500]

Memory Voltage Switching Frequency

Allows you to set the switching frequency of memory voltage regulator in MHz. Use the <+> or <-> to adjust the value. The values range from 0.750MHz to 1.500MHz with an interval of 0.250MHz.
Configuration options: [Auto] [0.75000] - [1.50000]

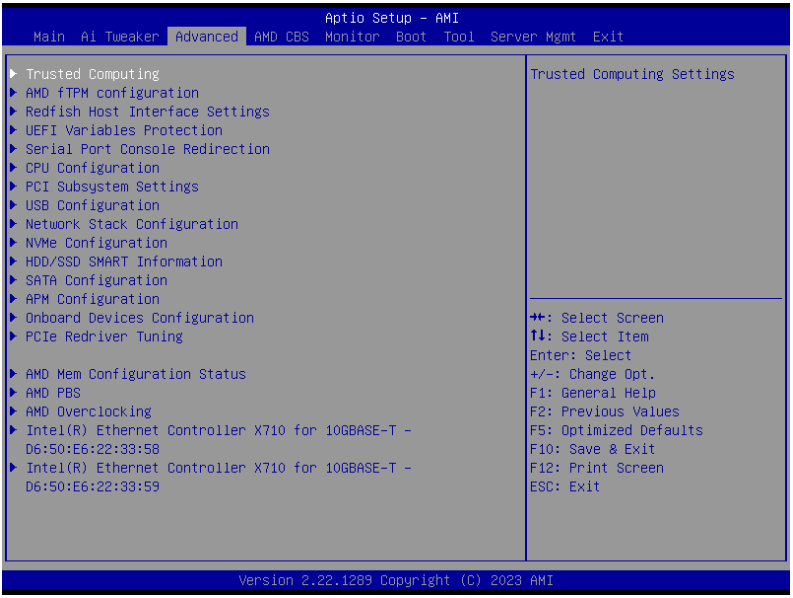
Memory Current Capability

Allows you to set the current capability for the Switching Regulators in Amps. Use the <+> or <-> to adjust the value. The values range from 0.125A to 7.875A with an interval of 0.125A.
Configuration options: [Auto] [0.12500] - [7.87500]

7. Advanced menu

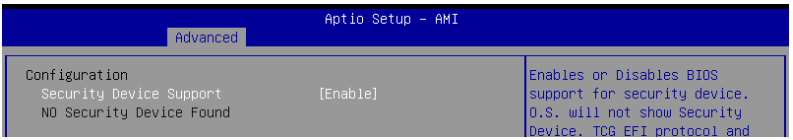
The Advanced menu items allow you to change the settings for the CPU and other system devices. Scroll down to display other BIOS items.

- Be cautious when changing the settings of the Advanced menu items. Incorrect field values can cause the system to malfunction.
- When overclocking, the warranty coverage declared by AMD official will be affected if you select **[Accept]** when the AMD warranty information statement appears. For more details please refer to the AMD official website.



7.1 Trusted Computing

The items in this menu allow you to configure the Trusted Computing settings.

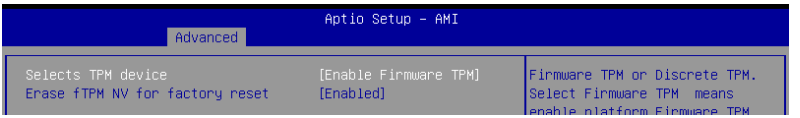


Security Device Support

Allows you to enable or disable the BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.
Configuration options: [Disable] [Enable]

7.2 AMD fTPM configuration

The items in this menu show the AMD fTPM configuration options.



Selects TPM device

Allows you to enable or disable Firmware TPM.

[Enable Firmware TPM] Enables platform Firmware TPM, disable Discrete TPM.

[Enable Discrete TPM] Enables Discrete TPM, disable platform Firmware TPM. Ensure to select this option if a Discrete TPM card is installed on your motherboard.

When **[Enable Discrete TPM]** is selected, fTPM will be disabled and all data saved on it will be lost.

Erase fTPM NV for factory reset

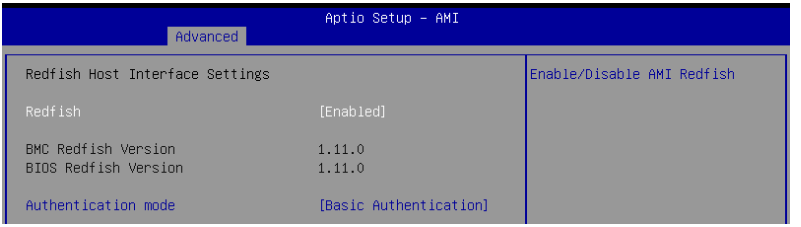
Allows you to enable or disable fTPM reset for newly installed CPUs.

[Disabled] Keep previous fTPM records and continue system boot, fTPM will not be enabled with the new CPU unless fTPM is reset (reinitialized). Swapping back to the old CPU may allow you to recover TPM related keys and data.

[Enabled] Reset fTPM, if you have Bitlocker or encryption-enabled system, the system will not boot without a recovery key.

7.3 Redfish Host Interface Settings

The items in this menu allow you to configure Redfish Host Interface Settings.



Redfish

Allows you to enable or disable AMI Redfish.
Configuration options: [Disabled] [Enabled]

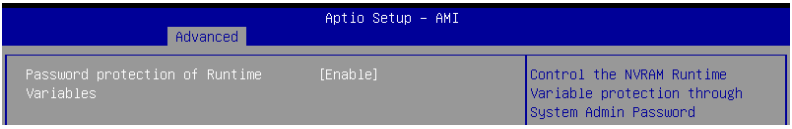
The following item appears only when **Redfish** is set to **[Enabled]**.

Authentication mode

Allows you to select the authentication mode.
Configuration options: [Basic Authentication] [Session Authentication]

7.4 UEFI Variables Protection

The items in this menu allow you to configure the NVRAM Runtime Variable Protection settings.

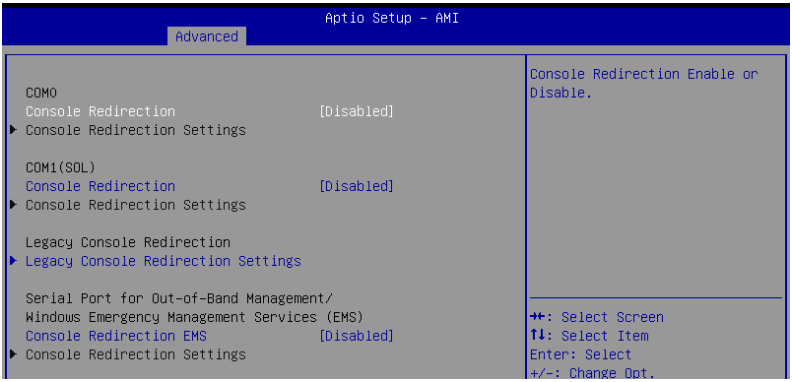


Password protection of Runtime Variables

Allows you to control the NVRAM Runtime Variable Protection through System Admin Password.
Configuration options: [Disable] [Enable]

7.5 Serial Port Console Redirection

The items in this menu allow you to configure serial port console redirection settings.



COM0 / COM1(SOL)

Console Redirection

Allows you to enable or disable the console redirection feature.
Configuration options: [Disabled] [Enabled]

The following item appears only when **Console Redirection** is set to **[Enabled]**.

Console Redirection Settings

These items become configurable only when you enable the Console Redirection item. The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

Terminal Type

Allows you to set the terminal type.

[VT100]	ASCII char set.
[VT100Plus]	Extends VT100 to support color, function keys, etc.
[VT-UTF8]	Uses UTF8 encoding to map Unicode chars onto 1 or more bytes.
[ANSI]	Extended ASCII char set.

Bits per second

Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Configuration options: [9600] [19200] [38400] [57600] [115200]

Data Bits

Configuration options: [7] [8]

Parity

A parity bit can be sent with the data bits to detect some transmission errors. [Mark] and [Space] parity do not allow for error detection. They can be used as an additional data bit.

[None]	None
[Even]	Parity bit is 0 if the num of 1's in the data bits is even.
[Odd]	Parity bit is 0 if num of 1's in the data bits is odd.
[Mark]	Parity bit is always 1.
[Space]	Parity bit is always 0.

Stop Bits

Stop bits indicate the end of a serial data packet. (A start bit indicates the beginning.) The standard setting is 1 stop bit. Communication with slow devices may require more than 1 stop bit.
Configuration options: [1] [2]

Flow Control

Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a "stop" signal can be sent to stop the data flow. Once the buffers are empty, a "start" signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
Configuration options: [None] [Hardware RTS/CTS]

VT -UTF8 Combo Key Support

This allows you to enable the VT -UTF8 Combination Key Support for ANSI/VT100 terminals.
Configuration options: [Disabled] [Enabled]

Recorder Mode

With this mode enabled only text will be sent. This is to capture Terminal data.
Configuration options: [Disabled] [Enabled]

Resolution 100x31

This allows you enable or disable extended terminal solution.
Configuration options: [Disabled] [Enabled]

Putty Keypad

This allows you to select the FunctionKey and Keypad on Putty.
Configuration options: [VT100] [LINUX] [XTERMR6] [SCO] [ESCN] [VT400]

Legacy Console Redirection Settings

Redirection COM Port

Allows you to select a COM port to display redirection of Legacy OS and Legacy OPROM Messages.
Configuration options: [COM0] [COM1(SOL)]

Resolution

This allows you to set the number of rows and columns supported on the Legacy OS.
Configuration options: [80x24] [80x25]

Redirection After POST

This setting allows you to specify if Bootloader is selected than Legacy console redirection.
Configuration options: [Always Enable] [Bootloader]

Serial Port for Out-of-Band Management/ Windows Emergency Management Services (EMS)

Console Redirection EMS

Allows you to enable or disable the console redirection feature.
Configuration options: [Disabled] [Enabled]

The following item appears only when **Console Redirection EMS** is set to **[Enabled]**.

Console Redirection Settings

The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

Out-of-Band Mgmt Port

Microsoft Windows Emergency Management Services (EMS) allow for remote management of a Windows Server OS through a serial port.
Configuration options: [COM0] [COM1(SOL)]

Terminal Type EMS

VT-UTF8 is the preferred terminal type for out-of-band management. The next best choice is VT100+, and then VT100. See above, in Console Redirection Settings page for more help with Terminal Type/Emulation.
Configuration options: [VT100] [VT100Plus] [VT-UTF8] [ANSI]

Bits per second EMS

Selects serial port transmission speed. The speed must be matched on the other side. Long or noisy lines may require lower speeds.
Configuration options: [9600] [19200] [57600] [115200]

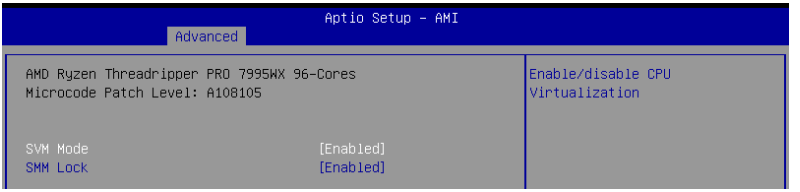
Flow Control EMS

Flow control can prevent data loss from buffer overflow. When sending data, if the receiving buffers are full, a “stop” signal can be sent to stop the data flow. Once the buffers are empty, a “start” signal can be sent to re-start the flow. Hardware flow control uses two wires to send start/stop signals.
Configuration options: [None] [Hardware RTS/CTS] [Software Xon/Xoff]

7.6 CPU Configuration

The items in this menu show the CPU-related information that the BIOS automatically detects. Scroll down to display other BIOS items.

The items in this menu may vary based on the CPU installed.



SVM Mode

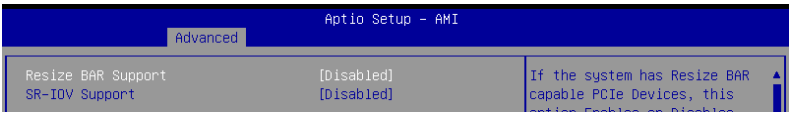
Allows you enable or disable CPU Virtualization.
Configuration options: [Disabled] [Enabled]

SMM Lock

Allows you enable or disable SMM Lock.
Configuration options: [Disabled] [Enabled]

7.7 PCI Subsystem Settings

The items in this menu allow you to configure PCI, PCI-X, and PCI Express settings.



Re-Size BAR Support

If the system has Resizable BAR capable PCIe Devices, this option enables or disables Resizable BAR Support (Only if System supports 64 bit PCI Decoding).
Configuration options: [Disabled] [Enabled]

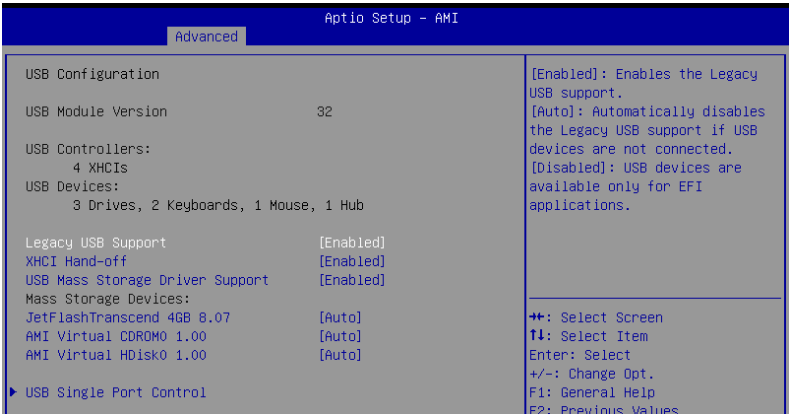
To enable Re-Size BAR Support for harnessing full GPU memory, please go to the **Boot** section and set **CSM(Compatibility Support Module)** to **[Disabled]**.

SR-IOV Support

Allows you to enable or disable Single Root IO Virtualization Support if the system has SR-IOV capable PCIe devices.
Configuration options: [Disabled] [Enabled]

7.8 USB Configuration

The items in this menu allow you to change the USB-related features.



The **Mass Storage Devices** item shows the auto-detected values. If no USB device is detected, the item shows **None**.

Legacy USB Support

[Enabled] Your system supports the USB devices in legacy operating systems.

[Disabled] USB devices are available only for EFI applications.

[Auto] Your system automatically detects the presence of USB devices at startup. If any USB devices are detected, the legacy USB support is enabled.

XHCI Hand-off

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

[Disabled] Support XHCI by XHCI drivers for operating systems with XHCI support.

[Enabled] Support XHCI by BIOS for operating systems without XHCI support.

USB Mass Storage Driver Support

Allows you to enable or disable USB Mass Storage Driver Support
Configuration options: [Disabled] [Enabled]

Mass Storage Devices:

Allows you to select the mass storage device emulation type for devices connected. **[Auto]** enumerates devices according to their media format. Optical drives are emulated as **[CD-ROM]**, drives with no media will be emulated according to a drive type.
Configuration options: [Auto] [Floppy] [Forced FDD] [Hard Disk] [CD-ROM]

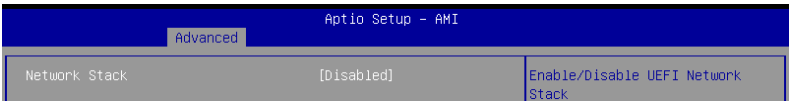
USB Single Port Control

Allows you to enable or disable the individual USB ports.

Refer to section **Motherboard layout** and **Rear I/O connection** in your motherboard's user guide for the location of the USB ports.

7.9 Network Stack Configuration

The items in this menu allow you to change the Network Stack Configuration.



Network stack

Allows you to disable or enable the UEFI network stack.
Configuration options: [Disabled] [Enabled]

The following items appear only when **Network Stack** is set to **[Enabled]**.

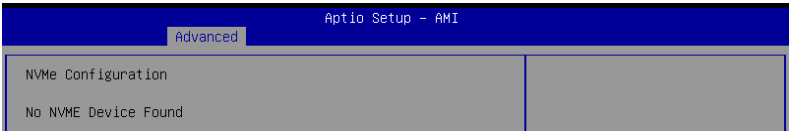
Ipv4/Ipv6 PXE Support

Allows you to enable or disable the Ipv4/Ipv6 PXE boot support.
Configuration options: [Disabled] [Enabled]

7.10 NVMe Configuration

This menu displays the NVMe controller and Drive information of the connected devices. You may press <Enter> on a connected NVMe device which appears in this menu to view more information on the NVMe device.

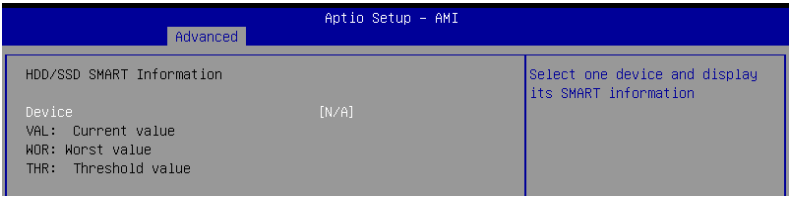
The options displayed in this menu may vary depending on the devices connected to your motherboard. Please refer to the BIOS of your motherboard for the actual settings and options.



7.11 HDD/SSD SMART Information

The items in this menu allow you to view the SMART information for connected storage devices.

The options displayed in this menu may vary depending on the devices connected to your motherboard. Please refer to the BIOS of your motherboard for the actual settings and options.

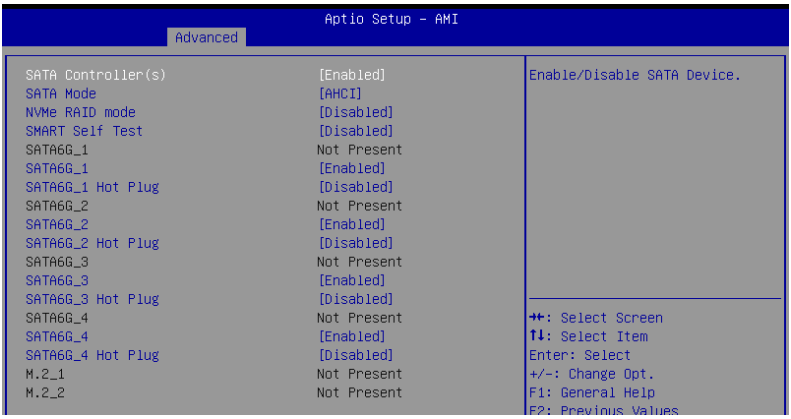


NVM Express devices do not support SMART information.

7.12 SATA Configuration

While entering Setup, the BIOS automatically detects the presence of SATA devices. The SATA Port items show **Empty** if no SATA device is installed to the corresponding SATA port. Scroll down to display the other BIOS items.

The settings and options of this menu may vary depending on your motherboard. Please refer to the BIOS of your motherboard for the actual settings and options.



SATA Controller(s)

Allows you to enable or disable the SATA Device.
Configuration options: [Disabled] [Enabled]

The following items appear only when **SATA Controller(s)** is set to **[Enabled]**.

SATA Mode

This item allows you to set the SATA configuration.

[AHCI]	Set to [AHCI] when you want the SATA hard disk drives to use the AHCI (Advanced Host Controller Interface). The AHCI allows the onboard storage driver to enable advanced Serial ATA features that increases storage performance on random workloads by allowing the drive to internally optimize the order of commands.
[RAID]	Set to [RAID] when you want to create a RAID configuration from the SATA hard disk drives.

NVMe RAID Mode

This item allows you to enable or disable the NVMe RAID mode.
Configuration options: [Disabled] [Enabled]

SMART Self Test

S.M.A.R.T. (Self-Monitoring, Analysis and Reporting Technology) is a monitoring system that shows a warning message during POST (Power-on Self Test) when an error occurs in the hard disks.
Configuration options: [Disabled] [Enabled]

SATA6G

Allows you to enable or disable the selected SATA port.
Configuration options: [Disabled] [Enabled]

SATA6G Hot Plug

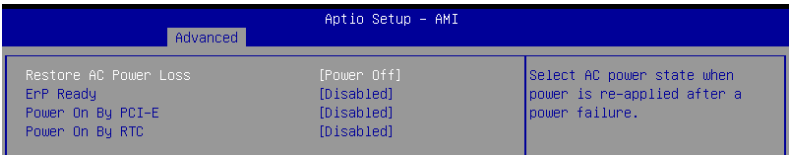
Designates this port as Hot Pluggable.
Configuration options: [Disabled] [Enabled]

M.2

Allows you to enable or disable the selected SATA port.
Configuration options: [Disabled] [Enabled]

7.13 APM Configuration

The items in this menu allow you to change the advanced power management settings.



Restore AC Power Loss

Allows your system to go to ON state, OFF state, or both states after an AC power loss. When setting your system to **[Last State]**, it goes to the previous state before the AC power loss.
Configuration options: [Power Off] [Power On] [Last State]

ErP Ready

Allows you to switch off some power at S4+S5 or S5 to get the system ready for ErP requirement. When set to **[Enabled]**, all other PME options are switched off. RGB LEDs and RGB/Addressable RGB Headers will also be disabled.
Configuration options: [Disabled] [Enabled (S4+S5)] [Enabled (S5)]

Power On By PCI-E

Allows you to enable or disable the Wake-on-LAN function of the onboard LAN controller or other installed PCI-E LAN cards.
Configuration options: [Disabled] [Enabled]

Power On By RTC

Allows you to enable or disable the RTC (Real-Time Clock) to generate a wake event and configure the RTC alarm date. When enabled, you can set the days, hours, minutes, or seconds to schedule an RTC alarm date.
Configuration options: [Disabled] [Enabled]

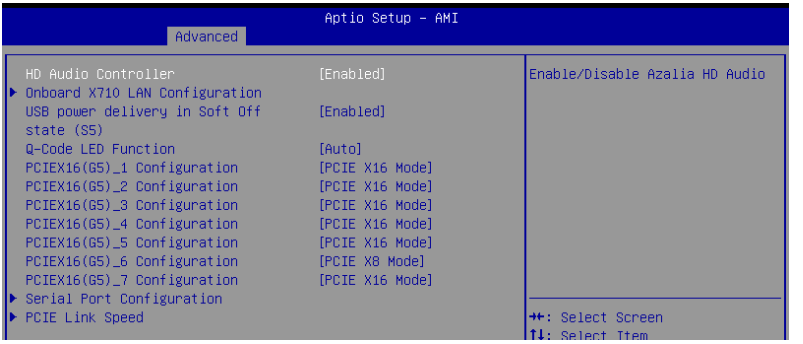
S3 Mode

Enabling this option might make the system unstable, as the least general power consumption is already over the specification of standard ATX PSU in S3 mode (5Vsb/3A).
Configuration options: [Disabled] [Enabled]

7.14 Onboard Devices Configuration

The items in this menu allow you to change the onboard devices settings. Scroll down to view the other BIOS items.

The settings and options of this menu may vary depending on your motherboard. Please refer to the BIOS of your motherboard for the actual settings and options.



HD Audio Controller

Allows you to enable or disable Azalia HD Audio.
Configuration options: [Disabled] [Enabled]

Onboard X710 LAN Configuration

Allows you to configure onboard X710 LAN configurations.

Intel X710 LAN1 and LAN2

LAN Enable

Allows you to enable or disable onboard LAN.
Configuration options: [Disabled] [LAN1, LAN2 Enabled]

USB power delivery in Soft Off state (S5)

Allows you to enable or disable USB power when your PC is in the S5 state.
Configuration options: [Disabled] [Enabled]

Wi-Fi Controller

Allows you to enable or disable the Wi-Fi Controller.
Configuration options: [Disabled] [Enabled]

Bluetooth Controller

Allows you to enable or disable the Bluetooth Controller.
Configuration options: [Disabled] [Enabled]

Q-Code LED Function

[Disabled]	Disable the Q-Code LED.
[POST Code Only]	Show POST (Power-On Self-Test) code on Q-Code LED.
[Auto]	Automatically display POST (Power-On Self-Test) code and CPU temperature on Q-Code LED.

PCIEX16 Configuration

[PCIE X16 Mode] PCIe slot runs at x16.

[PCIE RAID Mode] Up to 4 SSDs installed onto the Hyper M.2 X16 Series card can be detected.

Use **[PCIE RAID Mode]** when installing the Hyper M.2 X16 series card or other M.2 adapter cards. Installing other devices may result in a boot-up failure. The number of SSDs supported varies with the PCIe bifurcation abilities enabled by each processor.

PCIEX16 Configuration

[PCIE X8 Mode] PCIe slot runs at x8.

[PCIE RAID Mode] Up to 2 SSDs installed onto the Hyper M.2 X16 Series card can be detected.

Use **[PCIE RAID Mode]** when installing the Hyper M.2 X16 series card or other M.2 adapter cards. Installing other devices may result in a boot-up failure. The number of SSDs supported varies with the PCIe bifurcation abilities enabled by each processor.

Serial Port Configuration

This submenu allows you to set parameters for Serial Port.

This item will only function if there is a serial port (COM) connector on your motherboard.

Serial Port

Allows you to enable or disable the Serial port.
Configuration options: [Enabled] [Disabled]

The following item appears only when **Serial Port** is set to **[Enabled]**.

Change settings

Allows you to select an optimal setting for super IO device.
Configuration options: [IO=3F8h; IRQ=4] [IO=2F8h; IRQ=3] [IO=3E8h; IRQ=4] [IO=2E8h; IRQ=3]

PCIE Link Speed

This submenu allows you to set parameters for PCIE Link Speed.

PCIE Speed Control

Controls the PCIE speed mode for power optimization. This option allows user to choose between an optimized power consumption and performance-oriented power settings of a PCIe or M.2 slot.
Configuration options: [Disabled] [Enabled]

PCIEX16 Link Mode

Allows you to set the link speed for this PCIe slot.
Configuration options: [Auto] [GEN 1] [GEN 2] [GEN 3] [GEN 4] [GEN 5]

M.2 Link Mode

Allows you to set the link speed for M.2 Device.
Configuration options: [Auto] [GEN 1] [GEN 2] [GEN 3] [GEN 4] [GEN 5]

Chipset Link Mode

Allows you to set the link speed between CPU and Chipset.
Configuration options: [Auto] [GEN 1] [GEN 2] [GEN 3] [GEN 4]

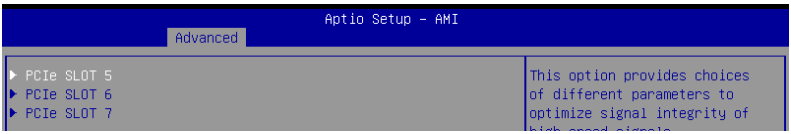
SLIMSAS Link Mode

Allows you to set the link speed for SLIMSAS Device.
Configuration options: [Auto] [GEN 1] [GEN 2] [GEN 3] [GEN 4]

7.15 PCIe Redriver Tuning

The items in this menu allow you to change different parameters to optimize signal integrity of high speed signals.

The settings and options of this menu may vary depending on your motherboard. Please refer to the BIOS of your motherboard for the actual settings and options.



PCIe SLOT

PCIe SLOT RX/TX

Gain

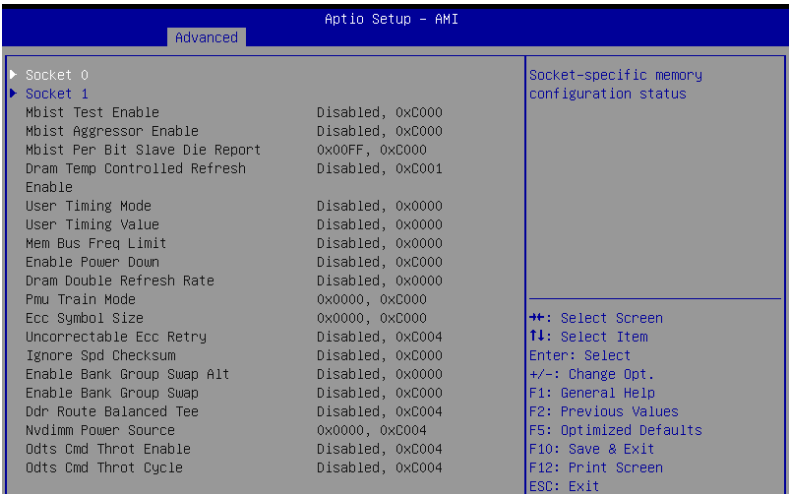
Allows you to set the Tuning Gain.
Configuration options: [11b] [10b] [01b] [00b]

EQ

Allows you to set the Tuning EQ.
Configuration options: [11111b] [11011b] [10111b] [10011b] [01111b] [01011b] [00111b] [00011b] [00010b] [00001b] [00000b]

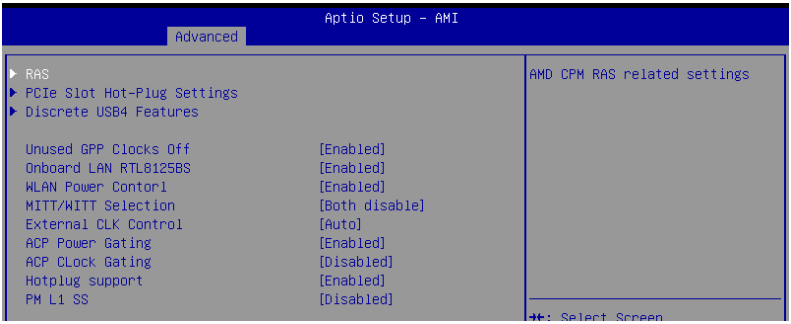
7.16 AMD Mem Configuration Status

The items in this menu display the memory configuration (initialized by ABL) status.



7.17 AMD PBS

The items in this menu display the memory configuration (initialized by ABL) status.



RAS

The items in this submenu allow you to configure AMD CPM RAS related settings.

RAS Periodic SMI Control

Allows you to enable or disable Periodic SMI for polling [MCA Threshold] error. Configuration options: [Disabled] [Enabled]

The following items appear only when **RAS Periodic SMI Control** is set to **[Enabled]**.

SMI Threshold

The [SMI Threshold] limits the number of [MCA Threshold and Deferred Error SMI source] per a Unit time (Defined by [SMI Scale]). (Default: 5 dec interrupts).
Configuration options: [0] - [65535]

SMI Scale

The [SMI Scale] defines the time scale. (Default: 1000 dec).
Configuration options: [0] - [32767]

SMI Scale Unit

The [SMI Scale Unit] defines unit of time scale. (Default: ms).
Configuration options: [millisecond] [second] [minute]

SMI Period

The [SMI Period] defines the polling interval. (Default: 1000 dec, Maximum: 32767 dec, 0: Disable, Unit: ms).
Configuration options: [0] - [32767]

GHES Notify Type

Notification type for deferred/corrected errors.
Configuration options: [Polled] [SCI]

GHES UnCorr Notify Type

Notification type for uncorrected errors.
Configuration options: [Polled] [NMI]

PCIe GHES Notify Type

Notification type for PCIe corrected errors.
Configuration options: [Polled] [SCI]

PCIe GHES UnCorr Notify Type

Notification type for PCIe uncorrected errors.
Configuration options: [Polled] [NMI]

GHES Root Port Corr Err Mask Reg

Initialize the PCIe AER Corrected Error Mask register of Root Port.
Configuration options: [0] - [FFFFFFFF]

GHES Root Port UnCorr Err Mask Reg

Initialize the PCIe AER Uncorrected Error Mask register of Root Port.
Configuration options: [0] - [FFFFFFFF]

PCIe Root Port UnCorr Error Sev Reg

Initialize the PCIe AER Uncorrected Error Severity registers of Root Port.
Configuration options: [0] - [FFFFFFFF]

PCIe Device Corr Err Mask Reg

Initialize the PCIe AER Corrected Error Mask register of PCie Device.
Configuration options: [0] - [FFFFFFFF]

PCIe Device UnCorr Err Mask Reg

Initialize the PCIe AER Uncorrected Error Mask register of PCie Device.
Configuration options: [0] - [FFFFFFFF]

PCIe Device UnCorr Err Sev Reg

Initialize the PCIe AER Uncorrected Error Severity registers of PCie Device.
Configuration options: [0] - [FFFFFFFF]

DRAM Hard Post Package Repair

Allows you to spare DRAM rows to replace malfunctioning rows via an in-field repair mechanism.
Configuration options: [Disabled] [Enabled]

HEST DMC Structure Support

Allows you to enable or disable HEST DMC (Deferred Machine Check) Structure Support.
Configuration options: [Disabled] [Enabled]

CXL Error Report Support

Allows you to enable or disable CXL Error Reporting.
Configuration options: [Disabled] [Enabled]

PCIe Slot Hot-Plug Settings

The items in this submenu allow you to change Build time Defined PCIe Slot Hot-Plug Settings.

Reserved IO Resources Padding

Allows you to pad PCI I/O resources behind the bridge for Hot-Plug.
Configuration options: [Disabled] [4 K] [8 K] [16 K] [Auto]

Reserved Non-Prefetchable MMIO Resources Padding

Allows you to pad PCI Non-Prefetchable MMIO resources behind the bridge for Hot-Plug.
Configuration options: [Disabled] [1 M] [2 M] [4 M] [8 M] [16 M] [32 M] [64 M] [128 M] [Auto]

Alignment for Reserved Non-Prefetchable MMIO Resources Padding

Allows you to pad PCI Alignment for Reserved Non-Prefetchable MMIO Resources behind the bridge for Hot-Plug.
Configuration options: [Disabled] [1 M] [2 M] [4 M] [8 M] [16 M] [32 M] [64 M] [128 M] [Auto]

Reserved Prefetchable MMIO Resources Padding

Allows you to pad PCI Prefetchable MMIO Resources behind the bridge for Hot-Plug.
Configuration options: [Disabled] [1 M] [2 M] [4 M] [8 M] [16 M] [32 M] [64 M] [128 M] [256 M] [512 M] [1 G] [2 G] [4 G] [8 G] [Auto]

Alignment for Reserved Prefetchable MMIO Resources Padding

Allows you to pad PCI Alignment for Reserved Prefetchable MMIO Resources behind the bridge for Hot-Plug.
Configuration options: [Disabled] [1 M] [2 M] [4 M] [8 M] [16 M] [32 M] [64 M] [128 M] [256 M] [512 M] [1 G] [2 G] [4 G] [8 G] [Auto]

Discrete USB4 Features

Discrete USB4 Support

Allows you to enable or disable Discrete USB4 PCIe slot.
Configuration options: [Disabled] [Enabled]

The following items appear only when **Discrete USB4 Support** is set to **[Enabled]**.

PCIe Bus Number

Reserve Discrete USB4 PCIe Bus number per port (16 ~ 56).
Configuration options: [16] - [56]

PCIe Non-Prefetchable MMIO

Reserve Discrete USB4 PCIe Non-Prefetchable MMIO per port (256 ~ 4096 MB).
Configuration options: [256] - [4096]

PCIe Prefetchable MMIO

Reserve Discrete USB4 PCIe Prefetchable MMIO per port (256 ~ 16384 MB).
Configuration options: [256] - [16384]

ACPI D3 Support

Allows you to enable or disable Discrete USB4 ACPI D3 Support.
Configuration options: [Disabled] [D3Hot] [D3Cold]

XHCI Port0~1 Speed

Allows you to configure the Discrete USB4 XHCI Port0~1 Speed.
Configuration options: [Gen1x1] [Gen1x2] [Gen2x1] [Gen2x2]

Unused GPP Clocks Off

Allows you to enable or disable Unused GPP Clocks.
Configuration options: [Disabled] [Enabled]

Onboard LAN RTL8125BS

Allows you to enable or disable Onboard LAN RTL8125BS.
Configuration options: [Disabled] [Enabled]

WLAN Power Control

Allows you to enable or disable WLAN Power Control.
Configuration options: [Disabled] [Enabled]

MITT/WITT Selection

Configuration options: [MITT Only] [WITT Only] [Both disable]

External CLK Control

[Auto]	100Mhz CGPLL generated by default.
[eCLK0, GPP0-PCIe, GPP0-CPU]	External input thru GPP1.

- Switch APU clocks source mapping will get stuck immediately (post code: B0005A5A), manual press cold reset button to bypass.
- The following items appear only when **External CLK Control** is set to **[eCLK0, GPP0-PCIe, GPP0-CPU]**.

GPP0 SCC control

Allows you to enable or disable Spread-Spectrum on GPP0 (RC26012A OUT0) and PCIe Slots (RC26012A OUT0, 0).
Configuration options: [Enabled] [Disabled]

GPP0 CCLK/PCIe Base Frequency

Adjust external clock RC2612A, range from 100MHz ~ 140MHz, step 1MHz.
Configuration options: [100] - [140]

ACP Power Gating

Allows you to enable or disable ACP Power Gating.
Configuration options: [Disabled] [Enabled]

ACP Power Gating

Allows you to enable or disable ACP Clock Gating.
Configuration options: [Disabled] [Enabled]

Hotplug support

Allows you to enable or disable Hotplug support.
Configuration options: [Disabled] [Enabled]

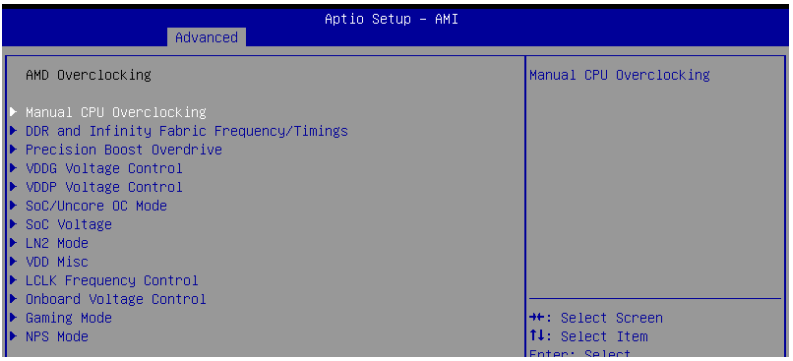
PM L1 SS

Allows you to enable PM L1 SS and ASPM L1 SS.
Configuration options: [Disabled] [L1.1] [L1.2] [L1.1_L1.2]

7.18 AMD Overclocking

The items in this menu shows the AMD Overclocking Setup page.

The configuration options for this section vary depending on the motherboard. Please refer to the BIOS of your motherboard for the actual settings and options.



Damage caused by use of your AMD processor outside of specification or in excess of factory settings are not covered by your system manufacturers warranty.

The following items appear only when **[Accept]** is selected for **AMD Overclocking**.

Manual CPU Overclocking

CPU Frequency

Specifies a custom CPU core frequency. Should be combined with a custom CPU voltage. Power saving features for idle cores (e.g. cc6 sleep) remain active.

VDDCR_CPU0~1 Voltage

Specifies a custom VDDCR_CPU0~1 voltage (mV). Stepping is 5mV. Voltage ranges allows to be set will be limited outside of LN2 mode. If in LN2 mode (and CPU temp is below -40C) the allowable range of settable voltages will be extended.
Configuration options: [0] - [2500]

CPU Core Count Control

CCD 00~11 Bit Map Down Core Control

Setting this item to 1 means core is enabled, setting this item to 0 means core is software down.

Bit Map Down Core Discard Changes

Discard changes.

Bit Map Down Core Apply Changes

Check and apply changes, need to make sure core number is equaled in each CCD.

SMT Control

Can be used to disable symmetric multithreading. To re-enable SMT, a POWER CYCLE is needed after selecting the **[Auto]** option.
Configuration options: [Auto] [Disable]

S3 is NOT SUPPORTED on systems where SMT is disabled.

Prochot VRM Throttling

Disabling Prochot will disable the VRMs ability to throttle the CPU when the voltage regulator is approaching its thermal limits.
Configuration options: [Auto] [Enable] [Disable]

Peak Current Control

Allows you to enable or disable PCC Feature.
Configuration options: [Auto] [Enable] [Disable]

DDR and Infinity Fabric Frequency/Timings

DDR Options

DDR Timing Configuration

Active Memory Timing Settings

Configuration options: [Auto] [Enabled]

The following items appear only when **Active Memory Timing Settings** is set to **[Enabled]**.

Memory Target Speed

Specifies the memory target speed in MT/s. The valid input is 2000 MT/s, 2400 MT/s, and range of 3200 MT/s ~ 12000 MT/s (stepping of 200 MT/s). The user input value will be rounded down to align with the stepping of 200 MT/s.

DDR SPD Timing

Tcl Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Tcl Ctrl** is set to **[Manual]**.

Tcl

Specifies the CAS Latency. Valid values: 0x16 ~ 0x40, with a stepping of 2. The value is in hex.

Trcd Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Trcd Ctrl** is set to **[Manual]**.

Trcd

Specifies the RAS# Active to CAS# Read Delay Time. Valid values: 0x8 ~ 0x3E with a stepping of 2. The value is in hex.

Trp Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Trp Ctrl** is set to **[Manual]**.

Trp

Specifies Row Precharge Delay Time. Valid values: 0x8 ~ 0x3E with a stepping of 2. The value is in hex.

Tras Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Tras Ctrl** is set to **[Manual]**.

Tras

Specifies Active to Precharge Delay Time. Valid values: 0x1E ~ 0x7E with a stepping of 2.

Trc Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Trc Ctrl** is set to **[Manual]**.

Trc

Specifies Active to Active/Refresh Delay Time. Valid values: 0x20 ~ 0xFF. The value is in hex.

Twr Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Twr Ctrl** is set to **[Manual]**.

Twr

Specifies the Minimum Write Recovery Time. Valid values: 0x30 ~ 0x60. The value is in hex.

Trfc1 Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Trfc1 Ctrl** is set to **[Manual]**.

Trfc1

Specifies the Refresh Recovery Delay Time (tRFC1). Valid values: 0x32 ~ 0xFFF. The value is in hex.

Trfc2 Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Trfc2 Ctrl** is set to **[Manual]**.

Trfc2

Specifies the Refresh Recovery Delay Time (tRFC2). Valid values: 0x32 ~ 0xFFF. The value is in hex.

TrfcSb Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **TrfcSb Ctrl** is set to **[Manual]**.

TrfcSb

Specifies the Refresh Recovery Delay Time (tRFCSB). Valid values: 0x32 ~ 0x7FF. The value is in hex.

Trtp Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Trtp Ctrl** is set to **[Manual]**.

Trtp

Specifies the Read CAS# to Precharge command delay time. Valid values: 0x5 ~ 0x1F. The value is in hex.

TrrdL Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TrrdL Ctrl** is set to **[Manual]**.

TrrdL

Specifies the Activate to Activate Delay Time, same bank group (tRRD_L). Valid values: 0x4 ~ 0x20. The value is in hex.

TrrdS Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TrrdS Ctrl** is set to **[Manual]**.

TrrdS

Specifies the Activate to Activate Delay Time, different bank group (tRRD_S). Valid values: 0x4 ~ 0x14. The value is in hex.

Tfaw Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **Tfaw Ctrl** is set to **[Manual]**.

Tfaw

Specifies the Four Activate Window Time. Valid values: 0x14 ~ 0x50. The value is in hex.

TwtrL Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TwtrL Ctrl** is set to **[Manual]**.

TwtrL

Specifies the Minimum Write to Read Time, the same bank group. Valid values: 0x8 ~ 0x30. The value is in hex.

TwtrS Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TwtrS Ctrl** is set to **[Manual]**.

TwtrS

Specifies the Minimum Write to Read Time, different bank group. Valid values: 0x2 ~ 0x10. The value is in hex.

DDR Non-SPD Timing

TrdrdScL Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TrdrdScL Ctrl** is set to **[Manual]**.

TrdrdScL

Specifies the CAS to CAS delay time, same bank group. Valid values: 0x1 ~ 0xF. The value is in hex.

TrdrdSc Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TrdrdSc Ctrl** is set to **[Manual]**.

TrdrdSc

Specifies the Read to Read turnaround timing in the same chipselect. Valid values: 0x1 ~ 0xF. The value is in hex.

TrdrdSd Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TrdrdSd Ctrl** is set to **[Manual]**.

TrdrdSd

Specifies the Read to Read turnaround timing in the same DIMM. Valid values: 0x1 ~ 0xF. The value is in hex.

TrdrdDd Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TrdrdDd Ctrl** is set to **[Manual]**.

TrdrdDd

Specifies the Read to Read turnaround timing in a different DIMM. Valid values: 0x1 ~ 0xF. The value is in hex.

TwrwrScL Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TwrwrScL Ctrl** is set to **[Manual]**.

TwrwrScL

Specifies the CAS to CAS Delay Time, same bank group. Valid values: 0x1 ~ 0x3F. The value is in hex.

TwrwrSc Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TwrwrSc Ctrl** is set to **[Manual]**.

TwrwrSc

Specifies the Write to Write turnaround timing in the same chipselect. Valid values: 0x1 ~ 0xF. The value is in hex.

TwrwrSd Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TwrwrSd Ctrl** is set to **[Manual]**.

TwrwrSd

Specifies the Write to Write turnaround timing in the same DIMM. Valid values: 0x1 ~ 0xF. The value is in hex.

TwrwrDd Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TwrwrDd Ctrl** is set to **[Manual]**.

TwrwrDd

Specifies the Write to Write turnaround timing in a different DIMM. Valid values: 0x1 ~ 0xF. The value is in hex.

Twrrd Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **Twrrd Ctrl** is set to **[Manual]**.

Twrrd

Specifies the Write to Read turnaround timing. Valid values: 0x1 ~ 0xF. The value is in hex.

Trdwr Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **Trdwr Ctrl** is set to **[Manual]**.

Trdwr

Specifies the Read to Write turnaround timing. Valid values: 0x1 ~ 0x1F. The value is in hex.

DDR BUS Configuration

Processor CA drive strengths

Specifies the Processor CA drive strengths.
Configuration options: [Auto] [120.0 Ohm] [60.0 Ohm] [40.0 Ohm] [30.0 Ohm]

Processor DQ drive strengths

Specifies the Processor DQ drive strengths.
Configuration options: [Auto] [High Impedance] [240 ohm] [120 ohm] [80 ohm] [60 ohm] [48 ohm] [40 ohm] [34.3 ohm]

Processor ODT impedance

Specifies the Processor ODT impedance.
Configuration options: [Auto] [High Impedance] [480 ohm] [240 ohm] [160 ohm] [120 ohm] [96 ohm] [80 ohm] [68.8 ohm] [60 ohm]

Dram DQ drive strengths

Specifies the DRAM DQ drive strengths.
Configuration options: [Auto] [48 ohm] [40 ohm] [34 ohm]

Dram ODT impedance RTT_NOM_WR

Specifies the DRAM ODT impedance RTT_NOM_WR.
Configuration options: [Auto] [RTT_OFF] [RZQ (240)] [RZQ/2 (120)] [RZQ/3 (80)] [RZQ/4 (60)] [RZQ/5 (48)] [RZQ/6 (40)] [RZQ/7 (34)]

Dram ODT impedance RTT_NOM_RD

Specifies the DRAM ODT impedance RTT_NOM_RD.
Configuration options: [Auto] [RTT_OFF] [RZQ (240)] [RZQ/2 (120)] [RZQ/3 (80)] [RZQ/4 (60)] [RZQ/5 (48)] [RZQ/6 (40)] [RZQ/7 (34)]

Dram ODT impedance RTT_WR

Specifies the DRAM ODT impedance RTT_WR.
Configuration options: [Auto] [RTT_OFF] [RZQ (240)] [RZQ/2 (120)] [RZQ/3 (80)] [RZQ/4 (60)] [RZQ/5 (48)] [RZQ/6 (40)] [RZQ/7 (34)]

Dram ODT impedance RTT_PARK

Specifies the DRAM ODT impedance RTT_PARK.
Configuration options: [Auto] [RTT_OFF] [RZQ (240)] [RZQ/2 (120)] [RZQ/3 (80)] [RZQ/4 (60)] [RZQ/5 (48)] [RZQ/6 (40)] [RZQ/7 (34)]

Dram ODT impedance DQS_RTT_PARK

Specifies the DRAM ODT impedance DQS_RTT_PARK.
Configuration options: [Auto] [RTT_OFF] [RZQ (240)] [RZQ/2 (120)] [RZQ/3 (80)] [RZQ/4 (60)] [RZQ/5 (48)] [RZQ/6 (40)] [RZQ/7 (34)]

DDR Controller Configuration

DDR Power Options

Power Down Enable

Allows you to enable or disable DDR power down mode.
Configuration options: [Disabled] [Enabled] [Auto]

Additional Memory Tweaks

RX DFE Taps

Allows you to specify the number of RX DFE taps, Value only applies when RX2D_DFE is enabled.
Configuration options: [Auto] [1 Tap] [2 Tap] [3 Tap] [4 Tap]

TX DFE Taps

Allows you to specify the number of TX DFE taps, Value only applies when TX2D_DFE is enabled.
Configuration options: [Auto] [1 Tap] [2 Tap] [3 Tap] [4 Tap]

Infinity Fabric Frequency and Dividers

Infinity Fabric Frequency and Dividers

Allows you to set Infinity Fabric Frequency (FCLK). Auto = FCLK = MCLK. Manual = FCLK must be less than MCLK for best performance in most cases. Latency penalties are incurred if FCLK and MCLK are mismatched, but sufficiently high MCLK can negate or overcome this penalty.
Configuration options: [Auto] [100 MHz] - [3000 MHz]

UCLK DIV1 MODE

Allows you to set UCLK DIV mode.
Configuration options: [Auto] [UCLK=MEMCLK] [UCLK=MEMCLK/2]

Precision Boost Overdrive

Precision Boost Overdrive

When this item is enabled, it allows the processor to run beyond defined values for PPT, VDD_CPU EDC, VDD_CPU TDC, VDD_SOC EDC, VDD_SOC TDC to the limits of the board, and allows it to boost at higher voltages for longer durations than default operation.
Configuration options: [Auto] [Disabled] [Enabled] [Advanced]

The following items appear only when **Precision Boost Overdrive** is set to **[Advanced]**.

PBO Limits

[Auto]	Loads AMD default socket power (PPT), electrically-limited VRM current (EDC), and thermally-limited VRM current (TDC) limits.
[Disable]	Disabled PBO limits.
[Motherboard]	Allows the processor to run according to increased PPT, EDC, and TDC limits defined by your motherboard.
[Manual]	Allows the processor to ignore AMD default limits for PPT, EDC, and TDC and instead use manual values (up to the maximum capabilities of the motherboard).

The following items appear only when **PBO Limits** is set to **[Manual]**.

PPT Limit [mW]

Adjust total CPU socket power delivery capability. Adjustable up to the limit supported bu your motherboard.

TDC Limit [mA]

Adjust peak current from your motherboard's CPU core VRM phases in thermally-limited scenarios. Adjustable up to the limit supported by you motherboard.

EDC Limit [mA]

Adjust peak current from your motherboard's CPU core VRM phases in electrically-limited scenarios. Adjustable up to the limit supported by you motherboard.

Precision Boost Overdrive Scalar Ctrl

Configuration options: [Auto] [Manual]

The following item appears only when **Precision Boost Overdrive Scalar Ctrl** is set to **[Manual]**.

Precision Boost Overdrive Scalar

Overrides the AMD default silicon health management to potentially achieve higher sustained frequencies under CPU load.
Configuration options: [1X] - [10X]

CPU Boost Clock Override

Increases (Positive) or Decreases (Negative) the maximum CPU frequency that may be automatically achieved by the CPU Boost Algorithm.
Configuration options: [Disabled] [Enabled (Positive)] [Enabled (Negative)]

The following item appears only when **CPU Boost Clock Override** is set to **[Enabled (Positive)]**.

Max CPU Boost Clock Override(+)

Increases the maximum CPU frequency that may be automatically achieved by the Precision Boost 2 algorithm. Use the <+> or <-> to adjust the value. The values range from 25 to 200 with an interval of 25.
Configuration options: [Auto] [25] - [200]

The following item appears only when **CPU Boost Clock Override** is set to **[Enabled (Negative)]**.

Max CPU Boost Clock Override(-)

Decreases the maximum CPU frequency that may be automatically achieved by the Precision Boost 2 algorithm. Use the <+> or <-> to adjust the value. The values range from 25 to 200 with an interval of 25.
Configuration options: [Auto] [25] - [200]

Platform Thermal Throttle Ctrl

Allows the user to decrease the maximum allowed processor temperature (celsius)
Configuration options: [Manual] [Auto]

The following item appears only when **Platform Thermal Throttle Ctrl** is set to **[Manual]**.

Platform Thermal Throttle Limit

Configuration options: [0] - [255]

Curve Optimizer

Curve Optimizer

Allows the user to shift the Voltage / Frequency (AVFS) curve to include higher voltages (positive values) or lower voltages (negative values). The larger the value entered the larger the magnitude of the voltage shift.
Configuration options: [Disable] [All Cores] [Per Core] [Per CCD]

The following items appear only when **Curve Optimizer** is set to **[All Cores]**.

All Core Curve Optimizer Sign

Determines the direction of the curve shift on all cores. Positive shifts the curve up to use higher voltages. Negative shifts the curve down to use lower voltages.
Configuration options: [Positive] [Negative]

All Core Curve Optimizer Magnitude

Determines the magnitude of the curve shift to be made (entered in whole numbers) the larger the value entered the larger the magnitude of the shift.
Configuration options: [0] - [50]

The following items appear only when **Curve Optimizer** is set to **[Per Core]**.

Core 0~95 Curve Optimizer Sign

Determines the direction of the curve shift on all cores. Positive shifts the curve up to use higher voltages. Negative shifts the curve down to use lower voltages.
Configuration options: [Positive] [Negative]

Core 0~95 Curve Optimizer Magnitude

Determines the magnitude of the curve shift to be made (entered in whole numbers) the larger the value entered the larger the magnitude of the shift.
Configuration options: [0] - [50]

The following items appear only when **Curve Optimizer** is set to **[Per CCD]**.

CCD 0~11 Curve Optimizer Sign

Determines the direction of the curve shift on all cores. Positive shifts the curve up to use higher voltages. Negative shifts the curve down to use lower voltages.
Configuration options: [Positive] [Negative]

CCD 0~11 Curve Optimizer Magnitude

Determines the magnitude of the curve shift to be made (entered in whole numbers) the larger the value entered the larger the magnitude of the shift.
Configuration options: [0] - [50]

VDDG Voltage Control

VDDG Voltage Control

VDDG represents voltage for the data portion of the Infinity Fabric. It is derived from the CPU SoC/Uncore Voltage (VDD_SOC). VDDG can approach but not exceed VDD_SOC.
Configuration options: [Auto] [Global VDDG Voltage Control] [Per-CCD VDDG Voltage Control]

The following items appear only when **VDDG Voltage Control** is set to **[Global VDDG Voltage Control]**.

Global VDDG CCD Voltage

VDDG CCD represents voltage for the data portion of the Infinity Fabric. It is derived from the CPU/SOC/Uncore Voltage (VDD_SOC). VDDG can approach but not exceed VDD_SOC.
Configuration options: [0] - [2047]

Global VDDG IOD Voltage

VDDG IOD represents voltage for the data portion of the Infinity Fabric. It is derived from the CPU/SOC/Uncore Voltage (VDD_SOC). VDDG can approach but not exceed VDD_SOC.
Configuration options: [0] - [2047]

The following items appear only when **VDDG Voltage Control** is set to **[Per-CCD VDDG Voltage Control]**.

CCD0-CCD VDDG Voltage

VDDG CCD represents voltage for the data portion of the Infinity Fabric. It is derived from the CPU/SOC/Uncore Voltage (VDD_SOC). VDDG can approach but not exceed VDD_SOC.
Configuration options: [0] - [2047]

CCD0-IOD VDDG Voltage

VDDG IOD represents voltage for the data portion of the Infinity Fabric. It is derived from the CPU/SOC/Uncore Voltage (VDD_SOC). VDDG can approach but not exceed VDD_SOC.
Configuration options: [0] - [2047]

VDDP Voltage Control

VDDP Voltage Control

Allows the user to adjust the VDDP voltage.

[Auto]	VDDP is system default.
[Manual]	Set voltage for the DDR bus signaling (PHY).

The following items appear only when **VDDP Voltage Control** is set to **[Manual]**.

VDDP Voltage Adjust

VDDP is a voltage for the DDR bus signaling (PHY), and it is dervied from your DRAM Voltage (VDDIO_Mem). As a result, VDDP voltage in mV can approach but not exceed your DRAM Voltage.
Configuration options: [0] - [2000]

SoC/Uncore OC Mode

SoC/Uncore OC Mode

Forces CPU SoC/Uncore components (e.g. Infinity Fabric, memory, and integrated graphics) to run at their maximum specified frequency at all times. May improve performance at the expense of idle power savings.
Configuration options: [Auto] [Enabled]

SoC Voltage

SoC Voltage

Specifies the SoC/Uncore voltage (VDD_SOC) in mV to support memory and Infinity Fabric overclocking. VDD_SOC also determines the GPU voltage on processors with integrated graphics. Voltage ranges allowed to be set will be limited outside of LN2 mode. If in LN2 mode (and CPU temp is below -40C) the allowance range of settable voltages will be extended.
Configuration options: [0] - [1300]

LN2 Mode

LN2 Mode

Enables settings that provide additional stability at extreme cold operatinf temperatures.
Configuration options: [Auto] [Disabled] [Enabled]

VDD Misc

VDD Misc Control

Allows the user to adjust the VDD Misc Voltage.

[Auto]	VDD MISC is set to system default.
[Manual]	Set voltage for the GMI PHY.

The following item appears only when **VDD Misc Control** is set to **[Manual]**.

VDD Misc Voltage

Specifies the VDD MISC Voltage in mV, definitely follow SVI3 type 2 Slave VID (500-5600mV, step 10mV).
Configuration options: [500] - [5600]

LCLK Frequency Control

LCLK Frequency Control

[Auto]	Use default settings.
[Manual]	Manually configure LCLK frequency.

The following item appears only when **LCLK Frequency Control** is set to **[Manual]**.

Maximum Frequency

Allows you to set the maximum LCLK frequency.
Configuration options: [889] - [2500]

Onboard Voltage Control

VDDIO Voltage Control

VDDIO Ctrl

Allows the user to adjust the VDDIO voltage.

[Auto]	Use the default VDDIO voltage.
[Manual]	Set DIMM VDD/VDDQ to synchronize to APU VDDIO.
[Separate]	Independent control of APU VDDIO, DIMM VDD/VDDQ.

Running VDDQ != VDD is non-standard and may cause memory stability issues. Take care that during ramp down and ramp up, the VDDQ-VDD voltage must be less than 200mV.

The following item appears only when **LCLK Frequency Control** is set to **[Manual]** or **[Separate]**.

DIMM VDD Adjust

Adjust DIMM Power Supply, stepping is 10mV. Range is from 800mV to 1430mV. Take care that during ramp down and ramp up, the VDDQ-VDD voltage must be less than 200mV.
Configuration options: [800] - [1430]

The following items appear only when **LCLK Frequency Control** is set to **[Separate]**.

DIMM VDDQ Adjust

Adjust DIMM DQ Power Supply, stepping is 10mV. Range is from 800mV to 1430mV. Take care that during ramp down and ramp up, the VDDQ-VDD voltage must be less than 200mV, and Vpp must always be equal to or greater than VDDQ.
Configuration options: [800] - [1430]

APU VDDIO Adjust

Adjust APO VDDIO, stepping is 2mV. Range is from 700mV to 2668mV.
Configuration options: [700] - [2668]

Enable Platform PMIC Control

When Enable Platform PMIC Control is enabled, the DDR PMIC voltages are not adjusted by processor FW, and may be adjusted directly by EC or other platform based mechanism.
Configuration options: [Auto] [Enable] [Disable]

VPP Voltage Control

VPP Ctrl

[Auto]	Use the default setting.
[Manual]	Manually specify the memory VPP Voltage.

The following item appears only when **VPP Ctrl** is set to **[Manual]**.

VPP Adjust

Adjust MEM VPP, stepping is 10mV. Range is from 1500mV to 2135mV.
Configuration options: [1500] - [2135]

Gaming Mode

Gaming Mode

Limitation:

1. Once user sets Gaming Mode as Enable, the CCD control option will not work anymore;
2. If user wants to use the CCD control under AOD, make sure Gaming Mode is set to disable.

Configuration options: [Disable] [Enable]

NPS Mode

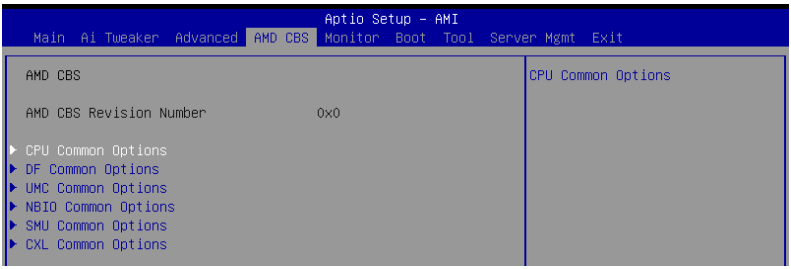
NUMA node per socket

Specifies the number of desired NUMA nodes per socket.
Configuration options: [Auto] [NPS1] [NPS2] [NPS4]

7.19 AMD CBS

The items in this menu shows the AMD Common BIOS Specifications.

The configuration options for this section vary depending on the motherboard. Please refer to the BIOS of your motherboard for the actual settings and options.



CPU Common Options

Thread Enablement

SMT Control

Can be used to disable symmetric multithreading. To re-enable SMT, a POWER CYCLE is needed after selecting the [Enable] option.
Configuration options: [Disable] [Enable] [Auto]

Performance

OC Mode

Select overclock operation modes.
Configuration options: [Normal Operation] [Customized]

Prefetcher settings

L1 Stream HW Prefetcher

Allows you to enable or disable L1 Stream HW Prefetcher.
Configuration options: [Disable] [Enable] [Auto]

L1 Stride Prefetcher

Uses memory access history of individual instructions to fetch additional lines when each access is a constant distance from the previous.
Configuration options: [Disable] [Enable] [Auto]

L1 Region Prefetcher

Uses memory access history to fetch additional lines when the data access for a given instruction tends to be followed by other data accesses.
Configuration options: [Disable] [Enable] [Auto]

L2 Stream HW Prefetcher

Allows you to enable or disable L2 Stream HW Prefetcher.
Configuration options: [Disable] [Enable] [Auto]

L2 Up/Down Prefetcher

Uses memory access history to determine whether to fetch the next or previous line for all memory accesses.
Configuration options: [Disable] [Enable] [Auto]

Core Watchdog

Core Watchdog Timer Enable

Allows you to enable or disable CPU Watchdog Timer.
Configuration options: [Disabled] [Enabled] [Auto]

The following item appears only when **Core Watchdog Timer Enable** is set to **[Enabled]**.

Core Watchdog Timer Interval

Allows you to select CPU Watchdog Timer interval.
Configuration options: [Auto] [39.68us] [80.64us] [162.56us] [326.4us] [654.08us] [1.309ms] [2.620ms] [5.241ms] [10.484ms] [20.970ms] [40.64ms] [82.53ms] [166.37ms] [334.05ms] [669.41ms] [1.340s] [2.681s] [5.364s]

RedirectForReturnDis

This option is from a workaround for GCC/C000005 issue for XV Core on CZ A0, setting MSRC001_1029 Decode Configuration (DE_CFG) bit 14 [DecfgNoRdrctForReturns] to 1.
Configuration options: [Auto] [1] [0]

Platform First Error Handling

Allows you to enable or disable PFEH, cloack individual banks, and mask deferred error interrupts from each bank.
Configuration options: [Enabled] [Disabled] [Auto]

Core Performance Boost

Allows you to disable Core Performance Boost.
Configuration options: [Disabled] [Auto]

Global C-state Control

Allows you to control IO based C-state generation and DF C-states.
Configuration options: [Disabled] [Enabled] [Auto]

PC6

Power Supply Idle Control.
Configuration options: [Low Current Idle] [Typical Current Idle] [Auto]

SEV-ES ASID Space Limit Control [Auto]

Allows you to select SEV-ES ASID Space Limit operation modes.
Configuration options: [Auto] [Manual]

The following item appears only when **SEV-ES ASID Space Limit Control** is set to **[Manual]**.

SEV-ES ASID Space Limit

SEV Vms using ASIDs below the SEV-ES ASID Space Limit must enable the SEV-ES feature. ASIDs from SEV-ES ASID Space Limit to (SEV ASID Count + 1) can only be used with SEV VMs. If this field is set to (SEV ASID Count + 1), all ASIDs are forced to be SEV-ES ASIDs. Hence, the valid values for this field is 1 - (SEV ASID Count + 1).
Configuration options: [1] - [520]

REP-MOV/STOS Streaming

Allow REP-MOV/STOS to use non-caching streaming store for large sizes.
Configuration options: [Disabled] [Enabled] [Auto]

Streaming Stores Control

Allows you to enable or disable the streaming stores functionality.
Configuration options: [Disabled] [Enabled] [Auto]

Local APIC MOde

Allows you to select local APIC operation modes.
Configuration options: [Compatibility] [xAPIC] [x2APIC] [Auto]

ACPI _CST C1 Declaration

Determines whether or not to declare the C1 state to the OS.
Configuration options: [Disabled] [Enabled] [Auto]

MCA error thresh enable

Allows you to enable MCA error thresholding.
Configuration options: [False] [True] [Auto]

The following item appears only when **MCA error thresh enable** is set to **[True]**.

MCA error thresh count

Effective error threshold count = 4095(0xFFF) - <this value> (e.g. the default value of 0xFF5 results in a threshold of 10)
Configuration options: [1] - [4095]

MCA FruText

Allows you to enable MCA FruText.
Configuration options: [False] [True]

SMU and PSP Debug Mode

When this item is set to **[Enabled]**, uncorrected errors detected by the PSP FW or SMU FW that should cause a cold reset, will hang and not restart the system.
Configuration options: [Disabled] [Enabled] [Auto]

PPIN Opt-in

Allows you to turn on PPIN feature.
Configuration options: [Disabled] [Enabled] [Auto]

SNP Memory (RMP Table) Coverage

When this item is set to **[Enabled]**, the ENTIE system memory is covered.
Configuration options: [Disabled] [Enabled] [Custom] [Auto]

The following item appears only when **SNP Memory (RMP Table) Coverage** is set to **[Custom]**.

Amount of Memory to Cover

Specify MB of System Memory to be covered in Hex.
Configuration options: [0] - [100000]

SMEE

Control secure memory enryption enable.
Configuration options: [Disable] [Enable] [Auto]

Action on BIST Failure

Allows you to set the action to take when a CCD BIST failure is detected.
Configuration options: [Do nothing] [Down-CCD] [Auto]

Enhanced REP MOVSB/STOSB (ERSM)

This item is set to 1 by default, but can be set to zero for analysis purposes as long as OS supports it.
Configuration options: [Disabled] [Enabled] [Auto]

Log Transparent Errors

This item is set to 1 by default, but can be set to zero for analysis purposes as long as OS supports it.
Configuration options: [Disabled] [Enabled] [Auto]

AVX512

Configuration options: [Disabled] [Enabled] [Auto]

MONITOR and MWAIT Disable

When this option is enabled, MONITOR, MWAIT, MONITORX, and MWAITX opcodes become invalid.
Configuration options: [Disabled] [Enabled] [Auto]

Enable Redirect Shutdown to HDT

Configuration options: [Enabled] [Auto]

Sync Flood on Uncorrected L2/L3 Errors

Trigger fatal error sync flood on uncorrected L2/L3 EXX errors.
Configuration options: [Disabled] [Enabled] [Auto]

SVM Enable

Allows you to enable or disable VM_CR[SvmeDisable].
Configuration options: [Enabled] [Disabled] [Auto]

SVM Lock

Allows you to enable or disable VM_CR[Lock].
Configuration options: [Enabled] [Disabled] [Auto]

DF Common Options

Memory Addressing

NUMA nodes per socket

Specifies the number of desired NUMA nodes per socket. Zero will attempt to interleave the two sockets together.
Configuration options: [NPS0] [NPS1] [NPS2] [NPS4] [Auto]

Memory interleaving

Allows for disabling memory interleaving.
Configuration options: [Disabled] [Auto]

NUMA nodes per socket will be honored regardless of this setting.

CXL Memory interleaving

Allows you to enable or disable CXL memory devices interleaving.
Configuration options: [Enabled] [Disabled] [Auto]

CXL Sublink interleaving

Allows you to enable or disable CXL sublink interleaving.
Configuration options: [Enabled] [Disabled] [Auto]

1TB remap

Attempt to remap DRAM out of the space just below the 1TB boundary. The ability to remap depends on DRAM configuration, NPS, and interleaving selection, and may not always be possible.
Configuration options: [Do not remap] [Attempt to remap] [Auto]

DRAM map inversion

Inverting the map will cause the highest memory channels to get assigned the lowest addresses in the system.
Configuration options: [Disabled] [Enabled] [Auto]

Location of private memory regions

Controls whether or not the private memory regions (PSP, SMU, and CC6) are at the top of DRAM or distributed. Note that distributed requires memory on all dies. Note that it will always be at the top of DRAM id some dies don't have memory regardless of this option's setting.
Configuration options: [Distributed] [Consolidated] [Consolidated to 1st DRAM pair] [Auto]

ACPI

ACPI SRAT L3 Cache as NUMA Domain

[Disabled]	Memory Addressing \ NUMA nodes per socket will be declared.
[Enabled]	Each CCX in the system will be declared as a separate NUMA domain.
[Auto]	Sets to the default option.

ACPI SLIT Distance Control

This option determines how the SLIT distances are declared.
Configuration options: [Manual] [Auto]

The following item appears only when **ACPI SLIT Distance Control** is set to **[Auto]**.

ACPI SLIT remote relative distance

Allows you to set the remote socket distance for 2P systems as near (2.8) or far (3.2).
Configuration options: [Near] [Far] [Auto]

The following items appear only when **ACPI SLIT Distance Control** is set to **[Manual]**.

ACPI SLIT same socket distance

Specify the distance to other physical domains within the same socket.
Configuration options: [10] - [255]

ACPI SLIT remote socket distance

Specify the distance to domains the remote socket.
Configuration options: [10] - [255]

ACPI SLIT local SLink distance

Specify the distance to an SLink domain on the same socket.
Configuration options: [10] - [255]

ACPI SLIT remote SLink distance

Specify the distance to an SLink domain on the other socket.
Configuration options: [10] - [255]

ACPI SLIT local inter-SLink distance

Specify the distance between two SLink domains on the same socket.
Configuration options: [10] - [255]

ACPI SLIT remote inter-SLink distance

Specify the distance between two SLink domains, each on a different socket.
Configuration options: [10] - [255]

Link

GMI encryption control

Allows you to control the GMI link encryption.
Configuration options: [Disabled] [Enabled] [Auto]

DF Watchdog Timer Interval

Allows you to set the Data Fabric watchdog timer interval.
Configuration options: [Auto] [41ms] [166ms] [334ms] [669ms] [1.34 seconds] [2.68 seconds] [5.36 seconds]

Disable DF to external downstream IP Sync Flood Propagation

Disables Error propagation to UMC or any downstream slaves eg. FCH. Use this to avoid reset in failure scenario.
Configuration options: [Sync flood disabled] [Sync flood enabled] [Auto]

Sync Flood Propagation to DF Components

Configuration options: [Sync flood disabled] [Sync flood enabled] [Auto]

Freeze DF module queues on error

Configuration options: [Disabled] [Enabled] [Auto]

System probe filter

Allows you to control whether or not the probe filter is enabled. Has no effect on parts where the probe filter is fuse disabled.
Configuration options: [Disabled] [Enabled] [Auto]

UMC Common Options

DDR Addressing Options

Chipselect Interleaving

Interleave memory blocks across the DRAM chip selects for node 0.
Configuration options: [Disabled] [Auto]

Address Hash Bank

Allows you to enable or disable bank address hashing.
Configuration options: [Disabled] [Enabled] [Auto]

Address Hash CS

Enable or disable CS address hashing.
Configuration options: [Auto] [Enabled] [Disabled]

Address Hash Rm

Enable or disable RM address hashing.
Configuration options: [Auto] [Enabled] [Disabled]

Address Hash Subchannel

Enable or disable Sub-channel address hashing.
Configuration options: [Auto] [Enabled] [Disabled]

BankSwapMode

Configuration options: [Auto] [Disabled] [Swap APU]

DDR Controller Configuration

This item allows you to configure DDR controller configuration.

DDR Power Options

Power Down Enable

Allows you to enable or disable DDR power down mode.
Configuration options: [Disabled] [Enabled] [Auto]

Sub Urgent Refresh Lower Bound

Configuration options: [Auto] [1] - [6]

Urgent Refresh Limit

Specifies the stored refresh limit required to enter urgent refresh mode. Constraint: SubUrgRefLowerBound <= UrgRefLimit Valid value: 6~1.
Configuration options: [Auto] [1] - [6]

DRAM Refresh Rate

DRAM refresh rate: 1.95us or 3.9us (default).
Configuration options: [3.9 usec] [1.95 usec]

Self-Refresh Exit Staggering

Tcksrx += (Trfc/n * (UMC_NUMBER % 3)) Selectable by CBS Option: Disable Staggering n = 1 <= Stagger Channels by ~270 ns, n=2 n=3 n=4... n=9 <= Stagger Channels By ~30 ns (Default).
Configuration options: [Auto] [Disabled] [n = 1] [n = 2] [n = 3] [n = 4] [n = 5] [n = 6] [n = 7] [n = 8] [n = 9]

Max PMIC Power On

Maximum number of DIMMs that can power on at the same time.
Configuration options: [1] - [FF]

Max PMIC Power On

Maximum number of DIMMs that can power on at the same time.
Configuration options: [1] - [FF]

PMIC Stagger Delay

Amount of time to wait between powering on DIMMs in milliseconds.
Configuration options: [0] - [99]

PMIC SWA/SWB VDD Core

Range is from 1000mV to 1200mV; default is set to 1100mV.
Configuration options: [1000] - [1200]

PMIC SWC VDDIO

Range is from 1000mV to 1200mV; default is set to 1100mV.
Configuration options: [1000] - [1200]

PMIC Fault Recovery

[Always]	PMIC will ignore previous boot errors. No channel disabled.
[Never]	PMIC disables the channel with errors from previous boot.
[Once]	PMIC will ignore the previous boot errors once. More than one channel will be disabled.

PMIC Operation Mode

Programmable Mode allows certain registers to be programmed after VR enable else they will be in secure mode.
Configuration options: [Secure Mode] [Programmable Mode]

DDR MBIST Options

This item allows you to configure DDR Memory MBIST.

MBIST Enable

Allows you to enable or disable Memory MBIST.
Configuration options: [Disabled] [Enabled] [Auto]

The following items appear only when **MBIST Enable** is set to **[Enabled]**.

MBIST Test Mode

Allows you to select the MBIST Test Mode - Interface Mode (Tests Single and Multiple CS transactions and Basic Connectivity) or Data Eye Mode (Measures Voltage vs. Timing).
Configuration options: [Interface Mode] [Data Eye Mode] [Both] [Auto]

MBIST Aggressors

Allows you to enable or disable Memory Aggressor test.
Configuration options: [Disabled] [Enabled] [Auto]

MBIST Per Bit Slave Die Reporting

Reports 2D Data Eye Results in ABL Log for each DQ, Chipselect, and Channel.
Configuration options: [Disabled] [Enabled] [Auto]

Data Eye

Pattern Select

Configuration options: [PRBS] [SSO] [Both]

Pattern Length

This token helps to determine the pattern length. The possible options are 3..C (input hex number, not decimal).
Configuration options: [3] - [C]

Aggressor Channel

This helps read the aggressors channels. If set to **[Enabled]**, you can read from one or more than one aggressor channel. The default is set to **[Disabled]**.
Configuration options: [Disabled] [1 Aggressor Channel] [3 Aggressor Channels] [7 Aggressor Channels]

Aggressor Static Lane Control

Allows you to control the Aggressor Static Lane Controls if enabled.
Configuration options: [Disabled] [Enabled]

The following items appear only when **Aggressor Static Lane Control** is set to **[Enabled]**.

Aggressor Static Lane Select Upper 32 bits

Static Lane Select for Upper 32 bits. The bit mask represents the bits to be read.
Configuration options: [0] - [99999999]

Aggressor Static Lane Select Lower 32 bits

Static Lane Select for Lower 32 bits. The bit mask represents the bits to be read.
Configuration options: [0] - [99999999]

Aggressor Static Lane Select ECC

Static Lane Select for ECC Lanes. The bit mask represents the bits to be read.
Configuration options: [0] - [9]

Aggressor Static Lane Value

Configuration options: [0] - [9]

Target Static Lane Control

Allows you to enable or disable Mbist Target Static Lane Control.
Configuration options: [Disabled] [Enabled]

The following items appear only when **Target Static Lane Control** is set to **[Enabled]**.

Target Static Lane Select Upper 32 bits

Static Lane Select for Upper 32 bits. The bit mask represents the bits to be read.
Configuration options: [0] - [99999999]

Target Static Lane Select Lower 32 bits

Static Lane Select for Lower 32 bits. The bit mask represents the bits to be read.
Configuration options: [0] - [99999999]

Target Static Lane Select ECC

Static Lane Select for ECC Lanes. The bit mask represents the bits to be read.
Configuration options: [0] - [9]

Target Static Lane Value

Configuration options: [0] - [9]

Worst Case Margin Granularity

Configuration options: [Per Chip Select] [Per Nibble]

Read Voltage Sweep Step Size

This option determines the step size for Read Data Eye voltage sweep.
Configuration options: [1] [2] [4]

Read Timing Sweep Step Size

This option supports step size for Read Data Eye.
Configuration options: [1] [2] [4]

Write Voltage Sweep Step Size

This option determines the step size for write Data Eye voltage sweep.
Configuration options: [1] [2] [4]

Write Timing Sweep Step Size

This option supports step size for write Data Eye.
Configuration options: [1] [2] [4]

Memory Healing BIST

Allows you to enable a full memory test. The testing will increase the boot time. BIOS mem BIST tests the full memory after training. Failing memory will be repaired using soft or hard PPR depending on the PPC configuration. The test will take 3 minutes per 16GN of installed memory. Self-Healing BIST runs the JEDEC DRAM self healing if the device supports the feature. The DRAM will do a hard repair for failing memory. The test will take 10 seconds per memory rank per channel.
Configuration options: [Disabled] [BIOS Mem BIST] [Self-Healing Mem BIST] [BIOS and Self-Healing Mem BIST]

The following items appear only when **Memory Healing BIST** is set to **[BIOS Mem BIST]**.

Mem BIST Test Select

Select the vendor specific tests to use with BIOS memory healing BIST.
Configuration options: [Vendor Tests Enabled] [Vendor Tests Disabled] [All Tests - All Vendors]

Mem BIST Post Package Repair Type

For DRAM errors found in the BIOS memory BIST select the repair type, soft, hard, or test only and do not attempt to repair.
Configuration options: [Soft Repair] [Hard Repair] [No Repairs - Test only]

DDR RAS

This item allows you to configure DDR RAS.

Data Poisoning

Enable poison data creation or uncorrectable DDR DRAM ECC errors and poison propagation to CPU cores and caches. Requires ECC memory. When FALSE, a fatal error event will occur on DDR ECC errors sets UMC_CH::EccCtrl[UcFatalEn] when MC_CH::EccCtrl[WrEccEn] is set.
Configuration options: [Disabled] [Enabled] [Auto]

DRAM Boot Time Post Package Repair

Allows you to enable or disable DRAM Boot Time Post Package Repair.
Configuration options: [Enable] [Disable]

RCD Parity

Allows you to enable or disable RCD command and address parity.
Configuration options: [Enabled] [Disabled] [Auto]

Max RCD Parity Error Replay

The values in hex, valid value 1 - 3F.
Configuration options: [1] - [3F]

Write CRC

Enable write CRC on DDR5 DRAM. Program to UMC::RecCtrl.RecEn[1].
Configuration options: [Auto] [Disabled] [Enabled]

The following item appears only when you set **Write CRC** to **[Enabled]**.

Max Write CRC Error Replay

Program to UMC::RecCtrl [MaxCrcRply], valid value: 1 - 3F. The values are in hex.
Configuration options: [1] - [3F]

Read CRC

Program to RecCtrl.RecEn[3].
Configuration options: [Auto] [Disabled] [Enabled]

The following item appears only when you set **Read CRC** to **[Enabled]**.

Max Read CRC Error Replay

Program to UMC::RecCtrl2 [MaxRdCrcRply], valid value: 1 - 3F. The values are in hex.
Configuration options: [1] - [3F]

Disable Memory Error Injection

Configuration options: [False] [True] [Auto]

ECC Configuration

DRAM ECC Symbol Size

Configuration options: [x4] [x16] [Auto]

DRAM ECC Enable

This option allows you to enable or disable DRAM ECC. Auto will set ECC to enable.
Configuration options: [Disabled] [Enabled] [Auto]

DRAM UECC Retry

This option allows you to enable or disable DRAM UECC Retry.
Configuration options: [Disabled] [Enabled] [Auto]

The following item appears only when you set **DRAM UECC Retry** to **[Enabled]**.

Max DRAM UECC Error Replay

Program to UMC::RecCtrl2 [MaxEccRply], valid value: 1 - 3F. The values are in hex.
Configuration options: [1] - [3F]

Memory Clear

Clear/Zero out DRAM range [DramScrubLimitAddr:DramScrubLimitAddr]. When this option is disabled, memory is not cleared after training. ECC DIMMs have memory clear enabled always. Non-ECC DIMMs can choose to disable/enable using this option.
Configuration options: [Enabled] [Disabled] [Auto]

Address XOR after ECC

In order to provide data integrity when data is returned from the wrong address, UMC will hash the data after ECC with the normalized address.
Configuration options: [Enabled] [Disabled] [Auto]

DRAM Scrubbers

DRAM ECS Mode

Setting this item to **[Auto]** will set ECS to Manual mode.
Configuration options: [AutoECS] [ManualECS] [Auto]

DRAM Redirect Scrubber Enable

Allows you to enable or disable Dram Redirect Scrubber.
Configuration options: [Disabled] [Enabled] [Auto]

DRAM Scrub Redirection Limit

Dram Redirect Scrub Redirection Limit: 0=8 scrubs, 1=4 scrubs, 2=2 scrubs, 3=1 scrubs.
Configuration options: [8 Scrubs] [4 Scrubs] [2 Scrubs] [1 Scrubs] [Auto]

DRAM Patrol Scrubber Enable

Allows you to enable or disable DRAM Patrol Scrubber. Setting this item to **[Auto]** will set this item to disabled.
Configuration options: [Disabled] [Enabled] [Auto]

DRAM Corrected Error Counter Enable

Allows you to configure the DRAM Corrected Error Counter function.
Configuration options: [Disable] [NoLeakMode] [LeakMode]

DRAM Corrected Error Counter Interrupt Enable

Allows you to enable SMI when DRAM Corrected Error Counter count exceeds the threshold value.
Configuration options: [False] [True]

DRAM Corrected Error Counter Leak Rate

Program Rate value for DRAM Corrected Error Counter function.
Configuration options: [0] - [1F]

DRAM Corrected Error Counter Start Count

Program starting count value for DRAM Corrected Error Counter function.
Configuration options: [0] - [FFFF]

PMIC Error Reporting

Allows you to enable support for PMMIC Error Reporting.
Configuration options: [False] [True] [Auto]

DDR Bus Configuration

This item allows you to configure DDR Bus Configuration.

Bus Configuration User Controls

Specify the mode for Bus configuration to Auto or Manual.
Configuration options: [Auto] [Manual]

The following item appears only when you set **Bus Configuration User Controls** to **[Manual]**.

RttNom_Wr

Configuration options: [Auto] [RTT_OFF] [RZQ (240)] [RZQ/2 (120)] [RZQ/3 (80)] [RZQ/4 (60)] [RZQ/5 (48)] [RZQ/6 (40)] [RZQ/7 (34)]

RttNom_Rd

Configuration options: [Auto] [RTT_OFF] [RZQ (240)] [RZQ/2 (120)] [RZQ/3 (80)] [RZQ/4 (60)] [RZQ/5 (48)] [RZQ/6 (40)] [RZQ/7 (34)]

RttPark

Configuration options: [Auto] [RTT_OFF] [RZQ (240)] [RZQ/2 (120)] [RZQ/3 (80)] [RZQ/4 (60)] [RZQ/5 (48)] [RZQ/6 (40)] [RZQ/7 (34)]

RttPark_Dqs

Configuration options: [Auto] [RTT_OFF] [RZQ (240)] [RZQ/2 (120)] [RZQ/3 (80)] [RZQ/4 (60)] [RZQ/5 (48)] [RZQ/6 (40)] [RZQ/7 (34)]

ProcODT

Configuration options: [Auto] [High Impedance] [480 ohm] [240 ohm] [160 ohm] [120 ohm] [96 ohm] [80 ohm] [68.6 ohm] [60 ohm] [53.3 ohm] [48 ohm] [43.6 ohm] [40 ohm] [36.9 ohm] [34.3 ohm] [32 ohm] [30 ohm] [28.2 ohm] [26.7 ohm] [25.3 ohm]

DRAM Data Drive Strength

Specifies the DRAM drive impedance.
Configuration options: [Auto] [48 ohm] [40 ohm] [34 ohm]

DDR Timing Configuration

This item allows you to configure DRAM timing configuration.

Damage caused by use of your AMD processor outside of specification or in excess of factory settings are not covered by your system manufacturers warranty.

The following items appear only when **[Accept]** is selected for **DRAM Timing Configuration**.

Active Memory Timing Settings

Configuration options: [Auto] [Enabled]

The following item appears only when you set **Active Memory Timing Settings** to **[Enabled]**.

Memory Target Speed

Specifies the memory target speed in MT/s. The valid input is 3200, 3600, 4000, 4400, 4800, 5200, 5600. Value is in decimal.

SPD Timing

Tcl Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Tcl Ctrl** is set to **[Manual]**.

Tcl

Specifies the CAS Latency. Valid values: 0x16 - 0x40, with a stepping of 2. The value is in hex.

Trcd Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Trcd Ctrl** is set to **[Manual]**.

Trcd

Specifies the RAS# Active to CAS# Read Delay Time. Valid values: 0x8 - 0x3E with a stepping of 2. The value is in hex.

Trp Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Trp Ctrl** is set to **[Manual]**.

Trp

Specifies Row Precharge Delay Time. Valid values: 0x8 - 0x3E with a stepping of 2. The value is in hex.

Tras Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Tras Ctrl** is set to **[Manual]**.

Tras

Specifies the minimum time in memory clock cycles from an activate command to a precharge command, both to the same bank. Valid values: 0x15 - 0x3A with a stepping of 2.

Trc Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Trc Ctrl** is set to **[Manual]**.

Trc

Specifies Active to Active/Refresh Delay Time. Valid values: 87h - 1Dh.

Twr Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Twr Ctrl** is set to **[Manual]**.

Twr

Specifies the Minimum Write Recovery Time. Valid values: 0xA - 0x64. The value is in hex.

Trfc1 Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **Trfc1 Ctrl** is set to **[Manual]**.

Trfc1

Specifies the Refresh Recovery Delay Time (tRFC1). Valid values: 3DEh - 3Ch.

Trfc2 Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **Trfc2 Ctrl** is set to **[Manual]**.

Trfc2

Specifies the Refresh Recovery Delay Time (tRFC2). Valid values: 3DEh - 3Ch.

TrfcSb Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TrfcSb Ctrl** is set to **[Manual]**.

TrfcSb

Specifies the Refresh Recovery Delay Time (tRFCSB). Valid values: 0x32 - 0x7FF. The value is in hex.

Non-SPD Timing

Tcwl Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **Tcwl Ctrl** is set to **[Manual]**.

Tcwl

Specifies the CAS Write Latency. Valid values: 0x9 - 0x16.

Trtp Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **Trtp Ctrl** is set to **[Manual]**.

Trtp

Specifies the Read CAS# to Precharge command delay time. Valid values: 0x5 - 0x0E.

TrrdL Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TrrdL Ctrl** is set to **[Manual]**.

TrrdL

Specifies the Activate to Activate Delay Time, same bank group (tRRD_L). Valid values: 0x4 - 0x0C. The value is in hex.

TrrdS Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **TrrdS Ctrl** is set to **[Manual]**.

TrrdS

Specifies the Activate to Activate Delay Time, different bank group (tRRD_S). Valid values: 0x4 - 0x0C. The value is in hex.

Tfaw Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Tfaw Ctrl** is set to **[Manual]**.

Tfaw

Specifies the Four Activate Window Time. Valid values: 6h - 36h. The value is in hex.

TwtrL Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **TwtrL Ctrl** is set to **[Manual]**.

TwtrL

Specifies the Minimum Write to Read Time, the same bank group. Valid values: 0x2 - 0xE.

TwtrS Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **TwtrS Ctrl** is set to **[Manual]**.

TwtrS

Specifies the Minimum Write to Read Time, different bank group. Valid values: 0x02 - 0x0E.

TrdrdScL Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **TrdrdScL Ctrl** is set to **[Manual]**.

TrdrdScL

Specifies the CAS to CAS delay time, same bank group. Valid values: 0x1 - 0xF.

TrdrdSc Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TrdrdSc Ctrl** is set to **[Manual]**.

TrdrdSc

Specifies the Read to Read turnaround timing in the same chipselect. Valid values: 0x1 - 0xF.

TrdrdSd Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TrdrdSd Ctrl** is set to **[Manual]**.

TrdrdSd

Specifies the Read to Read turnaround timing in the same DIMM. Valid values: 0x1 - 0xF.

TrdrdDd Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TrdrdDd Ctrl** is set to **[Manual]**.

TrdrdDd

Specifies the Read to Read turnaround timing in a different DIMM. Valid values: 0x1 - 0xF.

TwrwrScL Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TwrwrScL Ctrl** is set to **[Manual]**.

TwrwrScL

Specifies the CAS to CAS Delay Time, same bank group. Valid values: 3Fh - 1h.

TwrwrSc Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TwrwrSc Ctrl** is set to **[Manual]**.

TwrwrSc

Specifies the Write to Write turnaround timing in the same chipselect. Valid values: 0x1 - 0xF.

TwrwrSd Ctrl

[Auto] Follow default setting.
[Manual] Manually specify.

The following item appears only when **TwrwrSd Ctrl** is set to **[Manual]**.

TwrwrSd

Specifies the Write to Write turnaround timing in the same DIMM. Valid values: 0x1 - 0xF.

TwrwrDd Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **TwrwrDd Ctrl** is set to **[Manual]**.

TwrwrDd

Specifies the Write to Write turnaround timing in a different DIMM. Valid values: 0x1 - 0xF.

Twrrd Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Twrrd Ctrl** is set to **[Manual]**.

Twrrd

Specifies the Write to Read turnaround timing. Valid values: 0x1 - 0xF.

Trdwr Ctrl

[Auto]	Follow default setting.
[Manual]	Manually specify.

The following item appears only when **Trdwr Ctrl** is set to **[Manual]**.

Trdwr

Specifies the Read to Write turnaround timing. Valid values: 0x1 - 0x1F. The value is in hex.

DFI Channel Timing Configuration

RxDatChnDly

Configures the RX timing between memory controller and PHY. Higher value may enable increased memory frequency at the expense of increased latency.
Configuration options: [Auto] [1] [2]

TxDatChnDly

Configures the TX timing between memory controller and PHY. Higher value may enable increased memory frequency at the expense of increased latency.
Configuration options: [0] [1] [2] [3] [Auto]

TxCtrlChnDly

Configures the command timing between memory controller and PHY. Higher value may enable increased memory frequency at the expense of increased latency.
Configuration options: [0] [1] [Auto]

DDR Training Options

This item allows you to configure DDR Training Options.

DRAM PDA Enumerate ID Programming

Specify PDA Enumeration mode

[Auto]	Default setting.
[Toggling PDA enumeration mode]	Continuous DQS toggling PDA enumeration mode (default).
[Legacy PDA enumeration mode]	Legacy PDA enumeration mode.

DFE Read Training

Perform 2D Read Training with DFE on.
Configuration options: [Auto] [Enable] [Disable]

DDR Security

This item allows you to configure DDR Security.

TSME

Configuration options: [Auto] [Enabled] [Disabled]

AES

Configuration options: [AES-128] [AES-256]

Data Scramble

Configuration options: [Enabled] [Disabled] [Auto]

DDR Memory Features

This item allows you to configure DDR Memory Features.

Memory Context Restore

Allows you to configure the memory context restore mode. When enabled, DRAM re-training is avoided when possible and the POST latency is minimized.
Configuration options: [Auto] [Enabled] [Disabled]

DDR PHY Configuration

This item allows you to configure DDR PHY configurations.

DDR PHY PLL Bypass

Configuration options: [Auto] [Enabled] [Disabled]

DDR PHY PLL Bypass Frequency

[Auto]	Default settings.
[DDR-2000]	Enable PLL bypass for DDR-2000 and below.
[DDR-2400]	Enable PLL bypass for DDR-2400 and below.

NBIO Common Options

IOMMU

Configuration options: [Disabled] [Enabled] [Auto]

The following items appear only when **IOMMU** is set to **[Enabled]**.

Pre-boot DMA Protection

Allows you to enable or disable DMAr system protection during POST.
Configuration options: [Disabled] [Enabled] [Auto]

Kernal DMA Protection Indicator

Allows you to enable or disable DMA remap support in IVRS IVinfo Field.
Configuration options: [Disabled] [Enabled] [Auto]

DRTM Virtual Device Support

Configuration options: [Disabled] [Enabled] [Auto]

DRTM Memory Reservation

Allows you to enable or disable reservation of 128MB memory below Bottom IO for DRTM. This option is required for Secured-Core Server functionality.
Configuration options: [Disabled] [Enabled] [Auto]

ACS Enable

AER must be enabled for ACS enable to work.
Configuration options: [Enable] [Disabled] [Auto]

PCIe ARI Support

Enables Alternative Routing-ID Interpretation.
Configuration options: [Disable] [Enable] [Auto]

PCIe ARI Enumeration

ARI Forwarding enabled for each downstream port.
Configuration options: [Disable] [Enable] [Auto]

PCIe Ten Bit Tag Support

Allows you to enable PCIe ten bit tags for supported devices. Support is disabled if this option is set to **[Auto]**.
Configuration options: [Disable] [Enable] [Auto]

NBIO RAS Common Options

NBIO RAS Control

Configuration options: [Disabled] [MCA] [Auto]

Egress Poison Severity High

Each bit set to 1 enables HIGH severity on the associated IOHC egress port. A bit of 0 indicates LOW severity.

Egress Poison Severity Low

Each bit set to 1 enables HIGH severity on the associated IOHC egress port. A bit of 0 indicates LOW severity.

NBIO SyncFlood Generation

This value may be used to mask SyncFlood caused by NBIO RAS options. When set to TRUE, SyncFlood from NBIO is masked. When set to FALSE, NBIO is capable of generating SyncFlood.
Configuration options: [Enabled] [Disabled] [Auto]

NBIO SyncFlood Reporting

This value may be used to enable SyncFlood reporting to APML. When set to TRUE, SyncFlood will be reported to APML. When set to FALSE, the reporting will be disabled.
Configuration options: [Disabled] [Enabled] [Auto]

Egress Poison Mask High

These set the enable mask for masking of errors logged in EGRESS_ POISON_STATUS. For each bit set to 1, errors are masked. For each bit set to 0, errors trigger response actions.

Egress Poison Mask Low

These set the enable mask for masking of errors logged in EGRESS_ POISON_STATUS. For each bit set to 1, errors are masked. For each bit set to 0, errors trigger response actions.

Uncorrected Converted to Poison Enable Mask High

These set the enable mask for masking of uncorrectable parity errors on internal arrays. For each bit set to 1, a system fatal error event is triggered for UCP errors on arrays associated with that egress port. For each bit set to 0, errors are masked.

Uncorrected Converted to Poison Enable Mask Low

These set the enable mask for masking of uncorrectable parity errors on internal arrays. For each bit set to 1, a system fatal error event is triggered for UCP errors on arrays associated with that egress port. For each bit set to 0, errors are masked.

System Hub Watchdog Timer

This value specifies the timer interval of the SYSHUB Watchdog Timer in milliseconds.

SLink Read Response OK

This value specifies whether SLINK read response errors are converted to an Okay response. When this value is set to TRUE, read response errors are converted to Okay responses with data of all FFs. When set to FALSE, read response errors are not converted.
Configuration options: [Enabled] [Disabled]

SLink Read Response Error Handling

This value specifies whether SLINK write response errors are converted to an Okay response. When this value is set to 0, write response errors will be logged in the MCA. When set to 1, write response errors will trigger an MCOMMIT error. When this value is set to 2, write response errors are converted to Okay responses.
Configuration options: [Enabled] [Trigger MCOMMIT Error] [Log Errors in MCA]

Log Poison Data from SLINK

This value specifies whether poison data propagated from SLINK will generate a deferred error. When this value is set to TRUE, deferred errors are enabled. When set to FALSE, errors are not generated.
Configuration options: [Enabled] [Disabled]

PCIe Aer Reporting Mechanism

This value selects the method of reporting AER errors from PCI Express. A value of 1 allows OS First handling of the errors through generation of a system control interrupt (SCI). A value of 2 allows Firmware First handling of the errors through generation of a system management interrupt (SMI).
Configuration options: [Firmware First] [OS First] [Auto]

Edpc Control

Configuration options: [Disabled] [Enabled] [Auto]

ACS RAS Request Value

Configuration options: [Direct Request Access Enabled] [Request Blocking Enabled] [Request Redirect Enabled] [Auto]

NBIO Poison Consumption

Configuration options: [Auto] [Enabled] [Disabled]

Sync Flood on PCIe Fatal Error

Configuration options: [Auto] [True] [False]

Enable AER Cap

Allows you to enable or disable Advanced Error Reporting Capability.
Configuration options: [Enable] [Disabled] [Auto]

Early Link Speed

Allows you to set Early Link Speed.
Configuration options: [Auto] [Gen1] [Gen2]

Hot Plug Handling mode

Allows you to control the Hot Plug Handling mode.
Configuration options: [OS First] [Firmware First] [System Firmware Intermediary] [Auto]

Presence Detect Select mode

Allows you to control the Presence Detect Select mode.
Configuration options: [OR] [AND] [Auto]

Data Link Feature Cap

Allows you to set Data Link Feature Capability.
Configuration options: [Enabled] [Disabled] [Auto]

CV test

Set this to **[Enabled]** to support running PCIECV tool. Selecting **[Auto]** will preserve h/w defaults.
Configuration options: [Auto] [Enabled] [Disabled]

SEV-SNP Support

Allows you to enable or disable support for Secure Encrypted Virtualization and Secure Nested Paging.
Configuration options: [Disable] [Enable]

Allow Compliance

When enabled, allows the PCIe RP to enter Polling.Compliance state.
Configuration options: [Auto] [Disable] [Enable]

SRIS

Configuration options: [Auto] [Disable] [Enable]

Multi Upstream Auto Speed Change

Defines the setting of this feature for all PCIe devices. When this option is set to **[Auto]**, the DXIO default setting of 0 for Gen1 and 1 for Gen2/3.
Configuration options: [Disabled] [Enabled] [Auto]

Multi Auto Speed Change on Last Rate

Force PCIe link training speed to last advertised for all ports.

[Disabled] Use highest data rate ever advertised.
[Enabled] Use last data rate advertised.
[Auto] Use default settings.

RTM Margining Support

Configuration options: [Auto] [Enable] [Disable]

NBIO NBIF AZ

Configuration options: [Disabled] [Enabled] [Auto]

PCIe loopback Mode

Allows you to enable or disable PcieLoopBackMode.
Configuration options: [Auto] [Disabled] [Enabled]

SMU Common Options

TDP Control

[Auto] Use the fused TDP.
[Manual] User can set customized TDP.

The following item appears only when **TDP Control** is set to **[Manual]**.

TDP

Allows you to set the sustained power limit [W].

PPT Control

[Auto] Use the fused PPT.
[Manual] User can set customized PPT.

The following item appears only when **PPT Control** is set to **[Manual]**.

PPT

Allows you to set the PPT [W].

TjMax Control

[Auto]	Use the fused TjMax.
[Manual]	User can set customized TjMax.

The following item appears only when **TjMax Control** is set to **[Manual]**.

TjMax

Allows you to set the TjMax [C] (Used for thermal throttling).

Determinism Control

[Auto]	Use default performance determinism settings.
[Manual]	User can set customize performance determinism settings.

The following item appears only when **Determinism Control** is set to **[Manual]**.

Determinism Enable

Configuration options: [disable performance determinism] [enable performance determinism]

Thermal Control

[Auto]	Use the default TctlMax.
[Manual]	User can set customized TctlMax.

The following item appears only when **Thermal Control** is set to **[Manual]**.

TjMax

Allows you to set the maximum operating temperature ['C] (IRM limit will be enforced).

xGMI Link Width Control

[Auto]	Use default xGMI link width controller settings.
[Manual]	User can set custom xGMI link width controller settings.

The following items appear only when **xGMI Link Width Control** is set to **[Manual]**.

xGMI Force Link Width Control

[Auto]	Use default settings.
[Unforce]	Do not force the xGMI to a fixed width.
[Force]	Force the xGMI link to the user specified width.

The following item appears only when **xGMI Force Link Width Control** is set to **[Force]**.

xGMI Force Link Width

[Auto]	Use default settings.
[0]	Force xGMI link width to x2.
[1]	Force xGMI link width to x8.

xGMI Max Link Width Control

[Auto]	Use default xGMI max supported link width.
[Manual]	User can set custom xGMI max link width.

The following item appears only when **xGMI Max Link Width Control** is set to **[Manual]**.

xGMI Max Link Width

[Auto] Use default settings.
[0] Set max xGMI link width to x8.
[1] Set max xGMI link width to x16.

APBDIS

[Auto] Use default settings.
[0] Not APBDIS (mission mode)
[1] APBDIS

Power Profile Selection

Configuration options: [High Performance Mode] [Efficiency Mode] [Maximum IO Performance Mode]

BoostFmaxEn

[Auto] Use the default Fmax.
[Manual] User can set the boost Fmax.

The following item appears only when **BoostFmaxEn** is set to **[Manual]**.

BoostFmax

Allows you to specify the boost Fmax frequency limit to apply to all cores (MHz).
Configuration options: [0] - [9999]

DF PState Frequency Optimizer

Configuration options: [Auto] [Enabled] [Disabled]

DF PState Latency Optimizer

Configuration options: [Auto] [Enabled] [Disabled]

DF Cstates

Allows you to enable or disable DF C-states.
Configuration options: [Disabled] [Enabled] [Auto]

CPPC

Configuration options: [Disabled] [Enabled] [Auto]

CPPC Preferred Cores

[Auto] Use default settings.
[Enabled] CPPC highest capability register of each thread will have a different value to express the AMD recommended scheduling order to OS. CPPC must be enabled for this parameter to have effect.
[Disabled] Does not declare AMD preferred scheduling order to OS.

HSMP Support

This option allows you to enable or disable HSMP support.
Configuration options: [Disabled] [Enabled] [Auto]

SVI3 SVC Speed Control

Configuration options: [Auto] [Manual]

The following item appears only when **SVI3 SVC Speed Control** is set to **[Manual]**.

SVI3 SVC Speed

Configuration options: [50.00MHz] [40.00MHz] [26.67MHz] [20.00MHz] [16.00MHz] [13.33MHz] [10.00MHz] [8.00MHz] [5.00MHz]

3D V-Cache

Override of X3D technology.
Configuration options: [Auto] [Disable] [1 stack] [2 stack] [4 stack]

Infinity Fabric Frequency and Dividers

Configuration options: [Auto] [100 MHz] - [3000 MHz]

PCIe Speed PWM Control

Reduce link speed when devices are idle.
Configuration options: [Auto] [Dynamic link speed determined by Power Management functionality] [Static Target Link Speed (GEN4)] [Static Target Link Speed (GEN5)]

CXL Common Options

For an AVL of components that support CXL, please contact your sales representative.

CXL Control

Allows you to enable or disable CXL Control on all ports.
Configuration options: [Auto] [Enabled] [Disabled]

CXL Encryption

Configuration options: [Disabled] [Enabled]

CXL SPM

Set CXL memory as Special Purpose Memory.
Configuration options: [Disabled] [Enabled] [Auto]

CXL DVSEC Lock

Lock the CXL DVSEC.
Configuration options: [Disabled] [Enabled] [Auto]

Temp Gen5 Advertisement

Temp Gen5 Advertisementfor Alternate Protocol.
Configuration options: [Disabled] [Enabled] [Auto]

Sync Header Bypass

Configuration options: [Disabled] [Enabled] [Auto]

Speculative Reads to CXL

Configuration options: [Disabled] [Enabled] [Auto]

CXL RAS

CXL Protocol Error Reporting

Allows you to configure CXL Protocol Error reporting mechanism.
Configuration options: [Disabled] [SameAsPcieAer] [ForceAerFwFirstIfCxlPresent]

CXL Component Error Reporting

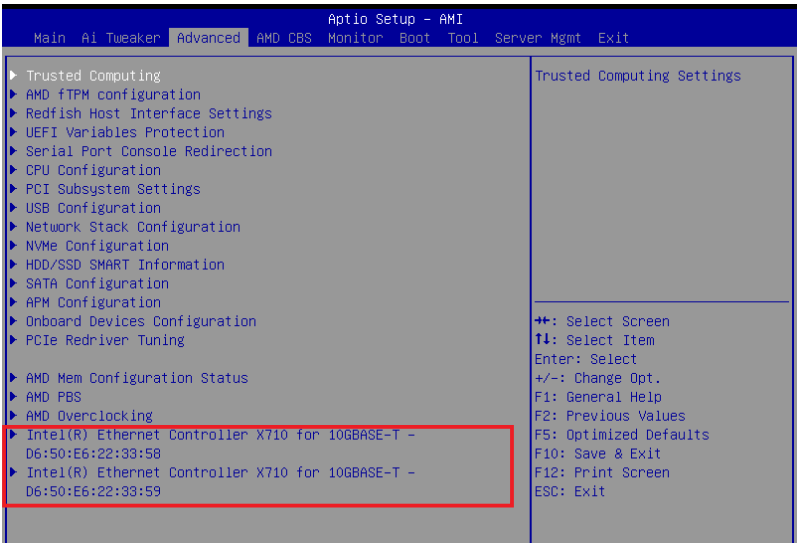
Allows you to configure CXL Component Error reporting mechanism.
Configuration options: [OS First] [FW-First]

Error Isolation CXL.mem

Configuration options: [Disabled] [Enabled] [Auto]

7.20 Third-party UEFI driver configurations

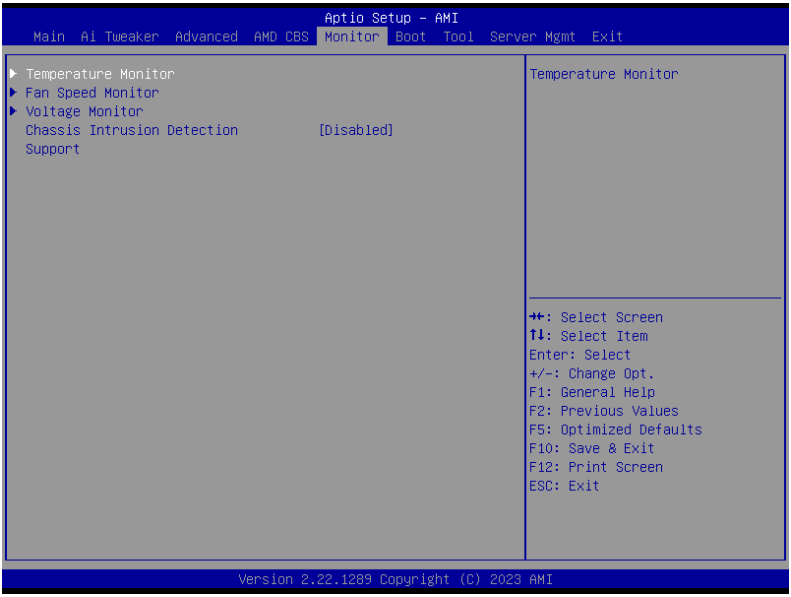
Additonal configuration options for third-party UEFI drivers installed to the system will appear in the bottom of the Advanced menu, in the section marked red in the screenshot below.



8. Monitor menu

The Monitor menu displays the system temperature/power status and fan speeds. Scroll down to display the other BIOS items.

The settings and options of this menu may vary depending on your motherboard. Please refer to the BIOS of your motherboard for the actual settings and options.



Temperature Monitor

MotherBoard Temperature, VRM Temperature, Chipset Temperature, T_Sensor Temperature, USB4 Thermistor Temperature, DIMM Temperature [xxx°C/xxx°F]

The onboard hardware monitor automatically detects and displays the temperatures for the different components. Select **[Ignore]** if you do not wish to display the detected temperatures.

Fan Speed Monitor

CPU Fan Speed, CPU Optional Fan Speed, Chassis Fan Speed, Water Pump+ Speed, VRM Heatsink Fan Speed, M.2 Fan Speed, USB4 Fan Speed [xxxx RPM]

The onboard hardware monitor automatically detects and displays the fan speeds in rotations per minute (RPM). If the fan is not connected to the motherboard, the field shows N/A. Select **[Ignore]** if you do not wish to display the detected speed.

Voltage Monitor

12V Voltage, 5V Voltage, 3.3V Voltage, CPU Core Voltage, CPU VSOC Voltage, CPU VDDIO / MC Voltage, DRAM VDD Voltage [x.xxx V]

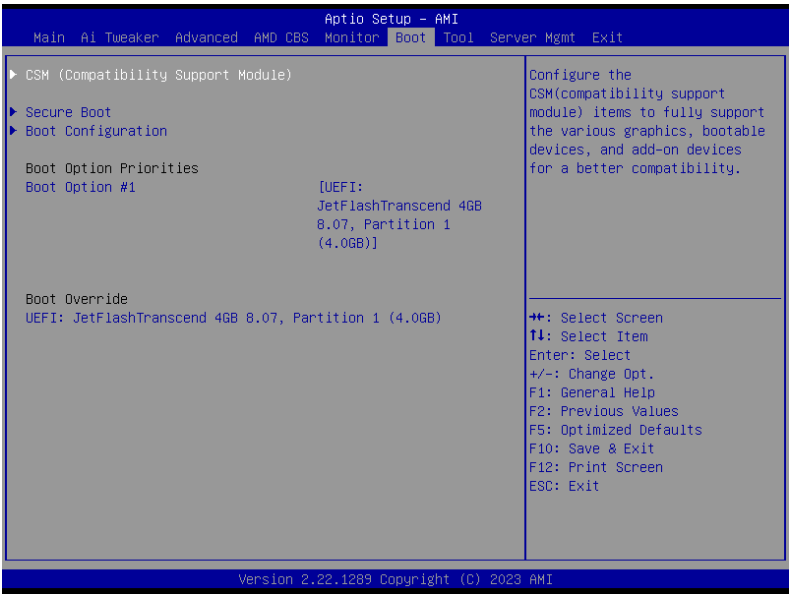
The onboard hardware monitor automatically detects the voltage output through the onboard voltage regulators. Select **[Ignore]** if you do not want to detect this item.

Chassis Intrusion Detection Support

Set this item to **[Enabled]** to enable the chassis intrusion detection function.
Configuration options: [Enabled] [Disabled]

9. Boot menu

The Boot menu items allow you to change the system boot options.



CSM (Compatibility Support Module)

Allows you to configure the CSM (Compatibility Support Module) items to fully support the various VGA, bootable devices and add-on devices for better compatibility.

Launch CSM will be set to **[Disabled]** and cannot be configured when using the integrated graphics.

Launch CSM

[Enabled] For better compatibility, enable the CSM to fully support the non-UEFI driver add-on devices or the Windows® UEFI mode.

[Disabled] Disable the CSM to fully support the non-UEFI driver add-on devices or the Windows® UEFI mode.

The following items appear only when **Launch CSM** is set to **[Enabled]**.

Boot Device Control

Allows you to select the type of devices that you want to boot.
Configuration options: [UEFI and Legacy OPROM] [Legacy OPROM only] [UEFI only]

Boot from Network Devices

Allows you to select the type of network devices that you want to launch.
Configuration options: [Ignore] [Legacy only] [UEFI only]

Boot from Storage Devices

Allows you to select the type of storage devices that you want to launch.
Configuration options: [Ignore] [Legacy only] [UEFI only]

Boot from PCI-E/PCI Expansion Devices

Allows you to select the type of PCI-E/PCI expansion devices that you want to launch.
Configuration options: [Ignore] [Legacy only] [UEFI only]

Secure Boot

Allows you to configure the Windows® Secure Boot settings and manage its keys to protect the system from unauthorized access and malwares during POST.

OS Type

[Windows UEFI Mode]	This item allows you to select your installed operating system. Execute the Microsoft® Secure Boot check. Only select this option when booting on Windows® UEFI mode or other Microsoft® Secure Boot compliant OS.
[Other OS]	Get the optimized function when booting on Windows® non-UEFI mode. Microsoft® Secure Boot only supports Windows® UEFI mode.

The Microsoft secure boot can only function properly on Windows UEFI mode.

Secure Boot Mode

This option allows you to select the Secure Boot mode from between Standard or Custom. In Custom mode, Secure Boot Policy variables can be configured by a physically present user without full authentication.
Configuration options: [Standard] [Custom]

The following item appears only when **Secure Boot Mode** is set to **[Custom]**.

Key Management

Install Default Secure Boot keys

Allows you to immediately load the default Security Boot keys, Platform key (PK), Key-exchange Key (KEK), Signature database (db), and Revoked Signatures (dbx). When the default Secure boot keys are loaded, the PK state will change from Unloaded mode to loaded mode.

Clear Secure Boot keys

This item appears only when you load the default Secure Boot keys. Allows you to clear all default Secure Boot keys.

Save all Secure Boot variables

Allows you to save all secure boot keys to a USB storage device.

PK Management

The Platform Key (PK) locks and secures the firmware from any permissible changes. The system verifies the PK before your system enters the OS.

Save To File

Allows you to save the PK to a USB storage device.

Set New key

Allows you to load the downloaded PK from a USB storage device.

Delete key

Allows you to delete the PK from your system. Once the PK is deleted, all the system's Secure Boot keys will not be active.
Configuration options: [Yes] [No]

The PK file must be formatted as a UEFI variable structure with time-based authenticated variable.

KEK Management

The KEK (Key-exchange Key or Key Enrollment Key) manages the Signature database (db) and Revoked Signature database (dbx).

Key-exchange Key (KEK) refers to Microsoft® Secure Boot Key-Enrollment Key (KEK).

Save to file

Allows you to save the KEK to a USB storage device.

Set New key

Allows you to load the downloaded KEK from a USB storage device.

Append Key

Allows you to load the additional KEK from a storage device for an additional db and dbx loaded management.

Delete key

Allows you to delete the KEK from your system.
Configuration options: [Yes] [No]

The KEK file must be formatted as a UEFI variable structure with time-based authenticated variable.

DB Management

The db (Authorized Signature database) lists the signers or images of UEFI applications, operating system loaders, and UEFI drivers that you can load on the single computer.

Save to file

Allows you to save the db to a USB storage device.

Set New key

Allows you to load the downloaded db from a USB storage device.

Append Key

Allows you to load the additional db from a storage device for an additional db and dbx loaded management.

Delete key

Allows you to delete the db file from your system.
Configuration options: [Yes] [No]

The db file must be formatted as a UEFI variable structure with time-based authenticated variable.

DBX Management

The dbx (Revoked Signature database) lists the forbidden images of db items that are no longer trusted and cannot be loaded.

Save to file

Allows you to save the dbx to a USB storage device.

Set New key

Allows you to load the downloaded dbx from a USB storage device.

Append Key

Allows you to load the additional dbx from a storage device for an additional db and dbx loaded management.

Delete key

Allows you to delete the dbx file from your system.
Configuration options: [Yes] [No]

The dbx file must be formatted as a UEFI variable structure with time-based authenticated variable.

Boot Configuration

Fast Boot

Allows you to enable or disable boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.
Configuration options: [Disabled] [Enabled]

Boot Logo Display

[Auto]	Automatically adjust the boot logo size for Windows requirements.
[Full Screen]	Maximize the boot logo size.
[Disabled]	Hide the logo during POST.

The following item appears only when **Boot Logo Display** is set to **[Auto]** or **[Full Screen]**.

Post Delay Time

Allows you to select a desired additional POST waiting time to easily enter the BIOS Setup. You can only execute the POST delay time during normal boot.
Configuration options: [0 sec] - [10 sec]

This feature only works when set under normal boot.

The following item appears only when **Boot Logo Display** is set to **[Disabled]**.

Post Report

Allows you to select a desired POST report waiting time or until ESC is pressed.
Configuration options: [1 sec] - [10 sec] [Until Press ESC]

Boot up NumLock State

Allows you to select the keyboard NumLock state.
Configuration options: [On] [Off]

Wait For 'F1' If Error

Allows your system to wait for the <F1> key to be pressed when error occurs.
Configuration options: [Disabled] [Enabled]

Option ROM Messages

[Force BIOS]	The Option ROM Messages will be shown during the POST.
[Keep Current]	Only the ASUS logo will be shown during the POST.

Interrupt 19 Capture

Enable this item to allow the option ROMs to trap the interrupt 19.
Configuration options: [Enabled] [Disabled]

AMI Native NVMe Driver Support

Allows you to enable or disable AMI Native NVMe driver.
Configuration options: [Disabled] [Enabled]

Boot Option Priorities

These items specify the boot device priority sequence from the available devices. The number of device items that appears on the screen depends on the number of devices installed in the system.

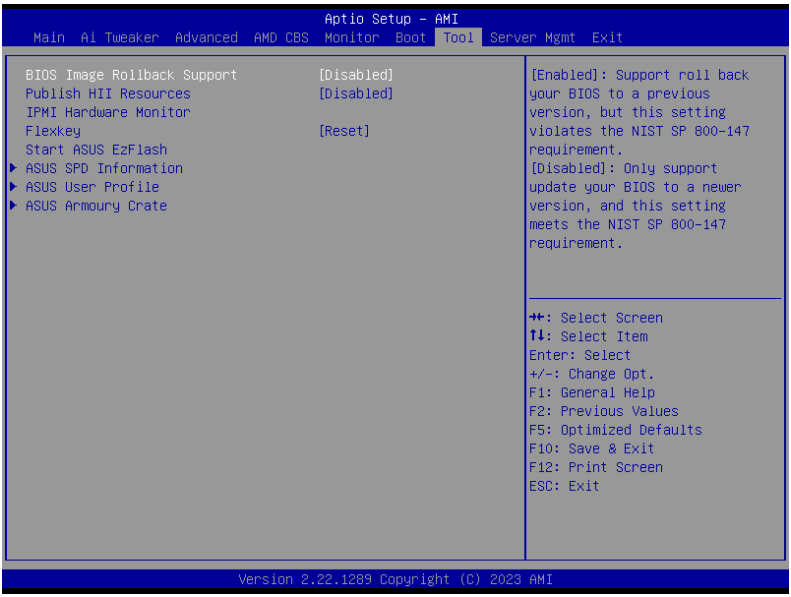
- To access Windows® OS in Safe Mode, press <F8 > after POST (Windows® 8 not supported).
- To select the boot device during system startup, press <F8> when ASUS Logo appears.

Boot Override

These item displays the available devices. The number of device items that appear on the screen depends on the number of devices installed in the system. Click an item to start booting from the selected device.

10. Tool menu

The Tool menu items allow you to configure options for special functions. Select an item then press <Enter> to display the submenu.



BIOS Image Rollback Support

[Enabled] Support roll back your BIOS to a previous version, but this setting violates the NIST SP 800-147 requirement.

[Disabled] Only support updating your BIOS to a newer version, and this setting meets the NIST SP 800-147 requirement.

Publish HII Resources

Configuration options: [Disabled] [Enabled]

IPMI Hardware Monitor

Allows you to view the IPMI Hardware Monitor when you press <Enter>.

Flexkey

Allows you to assign a different function to the Reset button (FlexKey).

[Reset] Reboots the system.

[DirectKey] Boot directly into the BIOS.

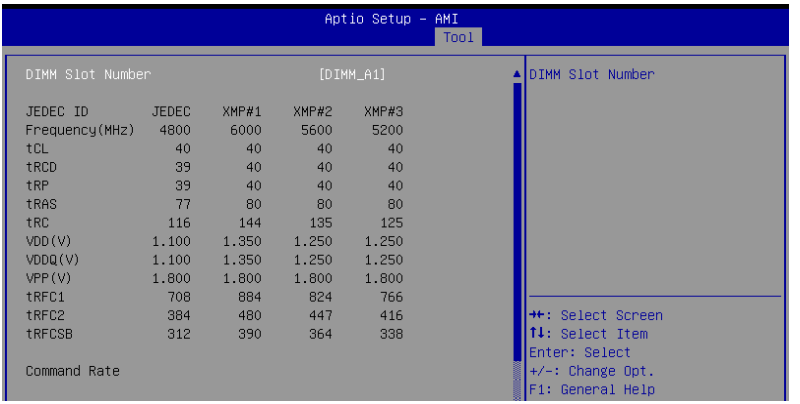
[Safe Boot] Force the system to reboot into the BIOS safe mode.

Start ASUS EzFlash

Allows you to run ASUS EzFlash BIOS ROM Utility when you press <Enter>. Refer to the **ASUS EzFlash Utility** section for details.

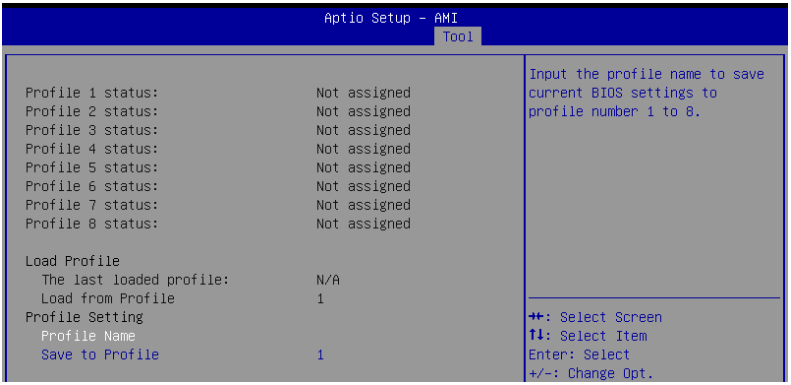
10.1 ASUS SPD Information

This item allows you to view the DRAM SPD information.



10.2 ASUS User Profile

This item allows you to store or load multiple BIOS settings.



Load from Profile

Allows you to load the previous BIOS settings saved in the BIOS Flash. Key in the profile number that saved your BIOS settings, press <Enter>, and then select **Yes**.

- DO NOT shut down or reset the system while updating the BIOS to prevent the system boot failure!
- We recommend that you update the BIOS file only coming from the same memory/ CPU configuration and BIOS version.

Profile Name

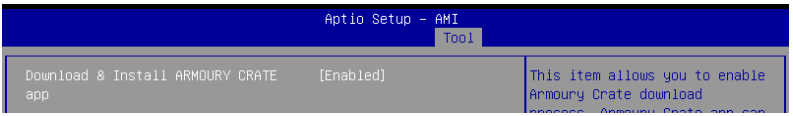
Allows you to key in a profile name.

Save to Profile

Allows you to save the current BIOS settings to the BIOS Flash, and create a profile. Key in a profile number from one to eight, press <Enter>, and then select **Yes**.

10.3 ASUS Armoury Crate

This item allows you to enable or disable downloading and installing of the Armoury Crate app in the Windows® OS. The Armoury Crate app can help you manage and download the latest drivers and utilities for your motherboard.



Download & Install ARMOURY CRATE app

Configuration options: [Disabled] [Enabled]

11. Server Mgmt menu

The Server Mgmt menu items allow you to configure IPMI settings.

OS Watchdog Timer

When this option is set to **[Enabled]** it starts a BIOS timer which can only be shut off by Management Software after the OS loads. Helps determine if the OS successfully loaded or follows the OS Boot Watchdog Timer policy.
Configuration options: [Enabled] [Disabled]

The following items appear only when **OS Watchdog Timer** is set to **[Enabled]**.

OS Wtd Timer Timeout

Enter a value between 1 and 30 min for OS Boot Watchdog Expiration, Not available if OS Boot Watchdog Timer is disabled.
Configuration options: [1] - [30]

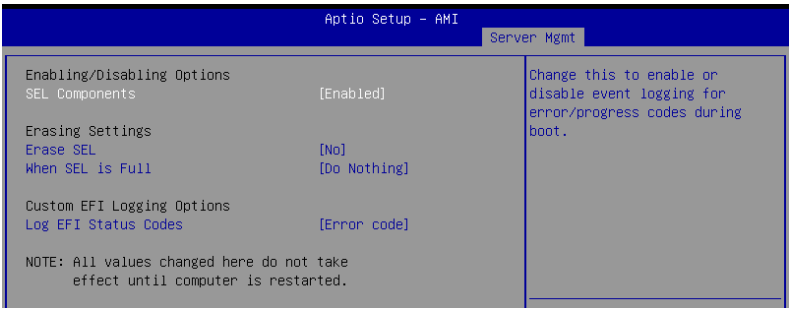
OS Wtd Timer Policy

This item allows you to configure the how the system should respond if the OS Boot Watch Timer expires.
Configuration options: [Do Nothing] [Reset] [Power Down] [Power Cycle]

11.1 System Event Log

Allows you to change the SEL event log configuration.

All values changed here do not take effect until computer is restarted.



SEL Components

Allows you to enable or disable event logging for error/progress codes during boot.
Configuration options: [Disabled] [Enabled]

The following items are configurable only when **SEL Components** is set to **[Enabled]**.

Erase SEL

Allows you to choose options for erasing SEL.
Configuration options: [No] [Yes, On next reset] [Yes, On every reset]

When SEL is Full

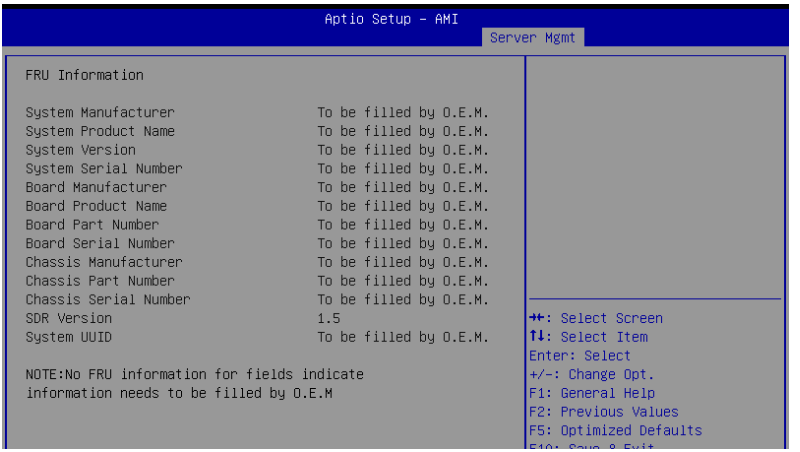
Allows you to choose options for reactions to a full SEL.
Configuration options: [Do Nothing] [Erase Immediately] [Delete Oldest Record]

Log EFI Status Codes

Disable the logging of EFI Status Codes or log only error code or only progress code or both.
Configuration options: [Disabled] [Both] [Error code] [Progress code]

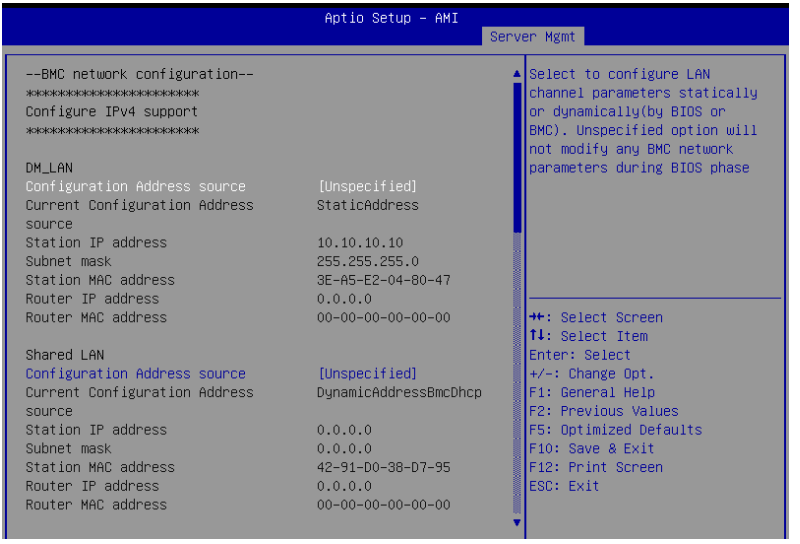
11.2 View FRU information

Press <Enter> to view FRU information.



11.3 BMC network configuration

The sub-items in this configuration allow you to configure the BMC network parameters.



Configure IPV4 support

DM_LAN / Shared LAN

Configuration Address source

This item allows you to configure LAN channel parameters statistically or dynamically (by BIOS or BMC). **[Unspecified]** option will not modify any BMC network parameters during BIOS phase.
Configuration options: [Unspecified] [Static] [DynamicBmcDhcp]

The following items are available only when **Configuration Address source** is set to **[Static]**.

Station IP address

Allows you to set the station IP address.

Subnet mask

Allows you to set the subnet mask. We recommend that you use the same Subnet Mask you have specified on the operating system network for the used network card.

Router IP Address

Allows you to set the router IP address.

Router MAC Address

Allows you to set the router MAC address.

Configure IPV6 support

DM_LAN / Shared LAN

IPV6 support

Allows you to enable or disable IPV6 support.
Configuration options: [Enabled] [Disabled]

The following items appear only when **IPV6 support** is set to **[Enabled]**.

Configuration Address source

Allows you to set the LAN channel parameters statically or dynamically (by BIOS or by BMC). **[Unspecified]** option will not modify any BMC network parameters during BIOS phase.
Configuration options: [Unspecified] [Static] [DynamicBmcDhcp]

The following items are available only when **Configuration Address source** is set to [Static].

Station IPV6 address

Allows you to set the station IPV6 address.

Prefix Length

Allows you to set the prefix length (maximum of Prefix Length is 128).

Configuration Router Lan1~2 Address source

Allows you to set the LAN channel parameters statically or dynamically (by BIOS or by BMC). **[Unspecified]** option will not modify any BMC network parameters during BIOS phase.
Configuration options: [Unspecified] [Static] [DynamicBmcDhcp]

The following items are available only when **Configuration Router Lan1 Address source** is set to **[Static]**.

IPV6 Router1 IP Address

Allows you to set the IPV6 Router1 IP address.

IPV6 Router1 Prefix Length Lan1~2

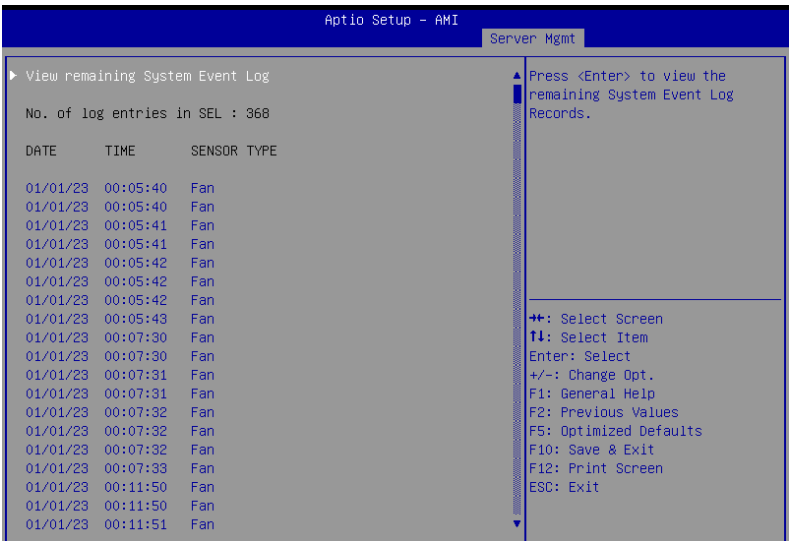
Allows you to set the IPV6 Router1 prefix length (maximum of Prefix Length is 128).

IPV6 Router1 Prefix Value Lan1~2

Allows you to set the IPV6 Router1 prefix value.

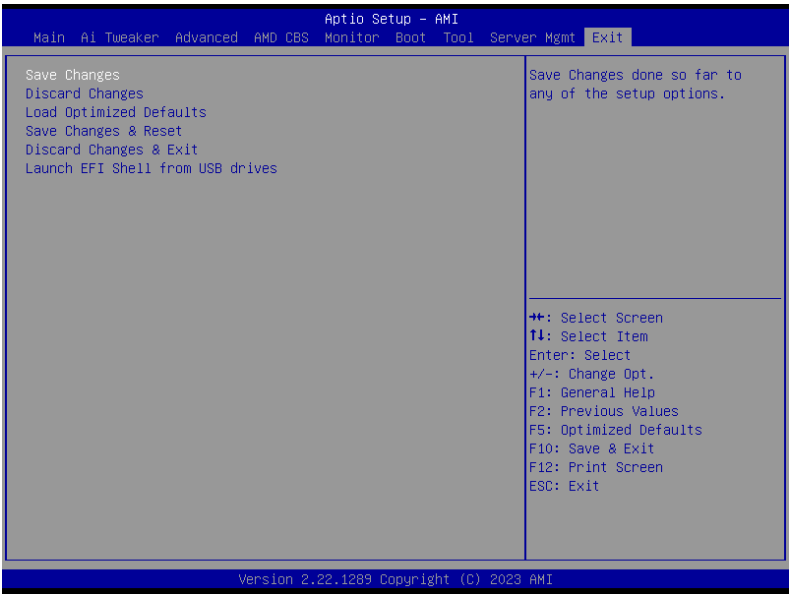
11.4 View System Event Log

This item allows you to view the system event log records.



12. Exit menu

The Exit menu items allow you to load the optimal default values for the BIOS items, and save or discard your changes to the BIOS items.



Save Changes

Save changes done so far to any of the setup options.

Discard Changes

Discard changes done so far to any of the setup options.

Load Optimized Defaults

Restores/loads the default values for all the setup options. When you select this option or if you press <F5>, a confirmation window appears. Select **OK** to load the default values.

Save Changes & Reset

Resets the system after saving the changes made. When you select this option or if you press <F10>, a confirmation window appears. Select **OK** to save changes and exit.

Discard Changes & Exit

This option allows you to exit the Setup program without saving your changes. When you select this option or if you press <Esc>, a confirmation window appears. Select **Yes** to discard changes and exit.

Launch EFI Shell from USB drives

This option allows you to attempt to launch the EFI Shell application (shellx64.efi) from one of the available filesystem devices.